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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC.,

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C03-4669 MJJ (EMC)

Case No. C03-2289 MJJ (EMC)

SUPPLEMENTAL DECLARATION OF DENISE M. DE MORY IN SUPPORT OF MOTIONS FOR SUMMARY JUDGMENT

I, Denise M. De Mory, declare as follows:

1. I am a partner at the law firm of Howrey LLP, counsel for Aeroflex Incorporated, Aeroflex Colorado Springs, AMI Semiconductor, Inc., Matrox Electronic Systems, Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. and Synopsys, Inc. (collectively, the "Defendants") in this action. The following declaration is based on my personal knowledge. If called upon to testify, I could and would competently testify to the matters set forth below.

2. The web pages in Exhibits 77-79 were all retrieved from Internet Archive at www.archive.org by undersigned counsel. Internet Archive is a well-known searchable library of archived web pages. Exhibits 77 and 78 are archived web pages from AMI's October 28, 1996 website. Exhibit 79 is an archived web page of UTMC's (i.e. Aeroflex's) November 21, 1996 website.

3. Attached as Exhibit 92 is a true and correct copy of the August 1986 Table of Contents of IEEE Design and test Computers journal;

4. Attached as Exhibit 93 is a true and correct copy of documents bates labeled KBSC 00002884 together with a translations and certification; [FILED UNDER SEAL]

5. Attached as Exhibit 94 is a true and correct copy of Ricoh Co. Ltd.'s Supplemental Privilege Log; [FILED UNDER SEAL]

6. Attached as Exhibit 95 is a true and correct copy of the August 16, 2006 Deposition Transcript of Joseph Colaianni; [FILED UNDER SEAL]

7. Attached as Exhibit 96 is a true and correct copy of the Amended Answer and Counterclaims of Defendant Aeroflex Incorporated to Amended Complaint for patent Infringement dated April 7, 2006;

8. Attached as Exhibit 97 is a true and correct copy of Defendants' Notice of Deposition of Ricoh Company, Ltd. Pursuant to Fed. R. Civ. P. 30(b)(6) dated March 2, 2006;

9. Attached as Exhibit 98 is a true and correct copy of the Customer Defendants' First Set of Request for Admissions;

10. Attached as Exhibit 99 is a true and correct copy of Electronic News webpage new article titled "Avant! Shakes Up Front End Design – Jupiter CAE software – Product Announcement"

11. Attached as Exhibit 100 is a true and correct copy of the May 26, 2006 email from J. Soccol to K. Brothers, et al. with attached letter and Federal Express air bill and delivery confirmation;

12. Attached as Exhibit 101 is a true and correct copy of webpage print out from cameo library;

13. Attached as Exhibit 102 is a true and correct copy of Exhibit 15 to Synopsys and Customer Defendants' Final Invalidity Contentions;

14. Attached as Exhibit 103 is a true and correct copy of Hearing Transcript from December 15, 2004;

15. Attached as Exhibit 104 is a true and correct copy of Webster's Ninth New Collegiate Dictionary page 334

16. Attached as Exhibit 105 is a true and correct copy of Webster's Ninth New Collegiate Dictionary page 688

17. Attached as Exhibit 106 is a true and correct copy of the June 7, 2006 Deposition Transcript of David Chiappini. [FILED UNDER SEAL]

Executed this 21st day of August, 2006, at San Francisco, California.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

/s/
Denise M. De Mory

IEEE
Design & Test of Comput

August 1986

THEME FEATURES

Circulation: *IEEE Design & Test of Computers* (ISSN 0740-7475) is published bimonthly by the IEEE Computer Society: IEEE Headquarters, 345 East 47th St., New York, NY 10017; IEEE Computer Society West Coast Office, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720. Annual subscription: $14.00 in addition to any IEEE group or society dues; nonmembers, $110.00. Single copy prices: members, $7.50; nonmembers, $15.00. This magazine is also available in microfiche form.
Undelivered copies: Send to 10662 Los Vaqueros Circle, Los Alamitos, CA 90720.
Postmaster: Send address changes to *IEEE Design & Test of Computers*, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. Second-class postage rates paid at New York, New York, and at additional mailing offices.

While unit manufacturing costs have steadily dropped in chip production, testing costs have remained high. A new breed of microcomputer-based testing equipment, such as the Logue-McDonald System 323i, aims to bring down test costs and reduce overall chip prices. For more details, see page 11.

Cover photo courtesy of Logue-McDonald

Cover design by Alexander Torres

Volume 3 Number 4 (ISSN 0740-7475)

CONFERENCES

...ARTMENTS

Coming in October:
Design for Testability

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MATROX GRAPHICS INC.,
MATROX INTERNATIONAL CORP.,
MATROX TECH, INC. and
AEROFLEX COLORADO SPRINGS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., and AEROFLEX COLORADO SPRINGS, INC.,

Defendants.

Case No. CV 03-04669 MJJ (EMC)

AMENDED ANSWER AND COUNTERCLAIMS OF DEFENDANT AEROFLEX INCORPORATED TO AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Defendant Aeroflex Incorporated ("Aeroflex") for its Amended Answer to the Amended Complaint and for its Counterclaims, hereby responds to the numbered paragraphs of the Amended Complaint filed by Ricoh Company, Ltd. ("Ricoh"), and in doing so denies the allegations of the Amended Complaint except as specifically stated:

PARTIES

1. Upon information and belief, Aeroflex admits that plaintiff Ricoh is a corporation organized under the laws of Japan and maintains its principal place of business at 3 -6 1-chome, Nakamagome, Tokyo, Japan.

2. Aeroflex admits that Aeroflex is a corporation organized under the laws of the State of Delaware, and maintains its principal place of business at 35 S. Service Road, Plainview, NY 11803. Aeroflex admits that Aeroflex has consented to the jurisdiction of Court for this action. Except as expressly admitted, Aeroflex denies the allegations of Paragraph 2 of the Amended Complaint.

3. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 3, and on that basis, denies those allegations.

4. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 4, and on that basis, denies those allegations.

5. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 5 of the Amended Complaint.

6. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 6, and on that basis, denies those allegations.

7. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 7, and on that basis, denies those allegations.

8. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 8, and on that basis, denies those allegations.

JURISDICTION

9. Aeroflex admits that plaintiff's claim purports to arise under the patent laws of the United States, Title 35, and more particularly under 35 U.S.C. §§ 271 *et. seq*. Except as expressly admitted, Aeroflex denies the allegations of Paragraph 9 of the Amended Complaint.

10. Aeroflex admits that the Court has subject matter jurisdiction over the allegations of patent infringement in the Amended Complaint pursuant to 28 U.S.C. §§ 1338(a) and 1331. Except as expressly admitted, Aeroflex denies the allegations of Paragraph 10 of the Amended Complaint.

11. Aeroflex admits that the Court has personal jurisdiction over Aeroflex. Except as expressly denied, Aeroflex denies the allegations of Paragraph 11 of the Amended Complaint.

VENUE

12. Aeroflex admits that venue is proper in this judicial district pursuant to 28 U.S.C. § 1391. Except as expressly admitted, Aeroflex denies the allegations of Paragraph 12 of the Amended Complaint.

FACTUAL BACKGROUND

13. Aeroflex admits that United States Patent No. 4,922,432 ("the '432 Patent") entitled "Knowledge Based Method and Apparatus for Designing Integrated Circuits using Functional Specifications," issued on May 1, 1990. Aeroflex admits that the '432 Patent names Hideaki Kobayashi and Masahiro Shindo as inventors. Aeroflex further admits that a copy of the '432 Patent is attached to the Amended Complaint as Exhibit 1. Except as expressly admitted, Aeroflex denies the allegations of Paragraph 13 of the Amended Complaint.

14. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 14, and on that basis, denies those allegations.

15. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 15, and on that basis, denies those allegations.

PATENT INFRINGEMENT

COUNT 1

16. Aeroflex repeats its responses to the allegations in Paragraphs 1 through 15 of the Amended Complaint.

17. Aeroflex denies each and every allegation in Paragraph 17 of the Amended Complaint.

18. Aeroflex denies each and every allegation in Paragraph 18 of the Amended Complaint.

19. Aeroflex denies each and every allegation in Paragraph 19 of the Amended Complaint.

20 Aeroflex denies each and every allegation in Paragraph 20 of the Amended Complaint..

21. Aeroflex denies each and every allegation in Paragraph 21 of the Amended Complaint.

COUNT 2

22. Aeroflex repeats its responses to the allegations in Paragraphs 1 through 15 of the Amended Complaint.

23. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 23, and on that basis, denies those allegations.

24. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 24, and on that basis, denies those allegations.

25. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 25, and on that basis, denies those allegations.

26. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 26, and on that basis, denies those allegations.

27. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 27, and on that basis, denies those allegations.

COUNT 3

28. Aeroflex repeats its responses to the allegations in Paragraphs 1 through 15 of the Amended Complaint.

29. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 29, and on that basis, denies those allegations.

30. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 30, and on that basis, denies those allegations.

31. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 31, and on that basis, denies those allegations.

32. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 32, and on that basis, denies those allegations.

33. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 33, and on that basis, denies those allegations.

COUNT 4

34. Aeroflex repeats its responses to the allegations in Paragraphs1 through 15 of the Amended Complaint.

35. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 35, and on that basis, denies those allegations.

36. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 36, and on that basis, denies those allegations.

37. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 37, and on that basis, denies those allegations.

38. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 38, and on that basis, denies those allegations.

39. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 39, and on that basis, denies those allegations.

COUNT 5

40. Aeroflex repeats its responses to the allegations in Paragraphs1 through 15 of the Amended Complaint.

41. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 41, and on that basis, denies those allegations.

42. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 42, and on that basis, denies those allegations.

43. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 43, and on that basis, denies those allegations.

44. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 44, and on that basis, denies those allegations.

45. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 45, and on that basis, denies those allegations.

COUNT 6

46. Aeroflex repeats its responses to the allegations in Paragraphs 1 through 15 of the Amended Complaint.

47. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 47, and on that basis, denies those allegations.

48. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 48, and on that basis, denies those allegations.

49. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 49, and on that basis, denies those allegations.

50. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 50, and on that basis, denies those allegations..

51. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 51, and on that basis, denies those allegations.

COUNT 7

52. Aeroflex repeats its responses to the allegations in Paragraphs 1 through 15 of the Amended Complaint.

53. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 53, and on that basis, denies those allegations.

54. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 54, and on that basis, denies those allegations.

55. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 55, and on that basis, denies those allegations.

56. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 56, and on that basis, denies those allegations.

57. Aeroflex lacks information sufficient to form a belief as to the truth of the allegations of Paragraph 57, and on that basis, denies those allegations.

DEFENSES

In further response to the Amended Complaint, Defendant Aeroflex asserts the following:

FIRST AFFIRMATIVE DEFENSE: INVALIDITY

58. The '432 Patent is invalid for failure to meet the requirements specified in Title 35 of the United States Code, including, but not limited to, 35 U.S.C. §§ 101, 102, 103, and 112 for one or more of the following reasons: (a) the inventor named in the '432 Patent did not invent or discover any new useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof within the meaning of 35 U.S.C. § 101; (b) the subject matter claimed in the '432 Patent was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before it was invented by the inventors named in the '432 Patent, as prohibited by 35 U.S.C. § 102(a); (c) the subject matter claimed in the '432 Patent was patented or described in a printed publication in this or a foreign country or was in public use or on sale in this country, more than one year prior to the filing of the application which resulted in the '432 Patent in the United States, as prohibited by 35 U.S.C. § 102(b); (d) the subject matter claimed in the '432 Patent was described in a United States patent based on an application filed in the United States or described in an application published prior to its invention by the inventors named in the '432 Patent, as prohibited by 35 U.S.C. § 102(e); (e) the inventor named in the '432 Patent did not invent the subject matter; (f) the subject matter claimed in the '432 Patent was invented in this country by another inventor, who did not abandon, suppress or conceal it, before its invention by the inventors named in the '432 Patent, as prohibited by 35 U.S.C. § 102(g); (g) the subject matter claimed in the '432 Patent would have been obvious, in view of the prior art, to a person having ordinary skill in the art at the time the invention was made under 35 U.S.C. § 103; and/or (h) the claims of the '432 Patent are invalid for failing to comply with 35 U.S.C. § 112, in that (i) the specification fails to contain a written description of the subject matter claimed in the `432 Patent and the manner and process of making and using it; (ii) the claims fail to particularly point out and distinctly claim a patentable invention, (iii) the claims are indefinite, (iv) the specification fails to enable one skilled in the art to practice the claimed invention, and/or (v) the specification fails to set forth the best mode contemplated by the named inventors for carrying out the alleged invention. Defendant reserves the right to amend this defense further, as additional information is developed through discovery or otherwise.

SECOND AFFIRMATIVE DEFENSE: NONINFRINGEMENT

59. Aeroflex has not used within the United Sates any processes that infringe any valid claim of the '432 Patent, either directly, indirectly, contributorily or otherwise, and has not induced others to infringe any valid claim of the '432 Patent.

60. Aeroflex has not offered to sell, sold, and/or imported within the United States any product made by a process that infringes any valid claim of the '432 Patent, either directly, indirectly, contributorily, or otherwise, and has not induced others to infringe any valid claim of the '432 Patent.

THIRD AFFIRMATIVE DEFENSE: LACHES

61. Between 1991 and 2001 Plaintiff Ricoh and Knowledge Based Silicon Corporation ("KBS") were co-assignees of the '432 patent. Pursuant to agreement, Ricoh paid the maintenance fees for the '432 patent. On information and belief, Ricoh and KBS coordinated all activities related to the '432 patent.

62. In or about 1991, KBS unsuccessfully tried to persuade Synopsys, Inc. ("Synopsys"), to license the '432 Patent. KBS subsequently abandoned those efforts, and instead developed and marketed products that were interoperable with Synopsys' Design Compiler product. Towards this end, KBS acquired a license to Design Compiler and received assistance from Synopsys to make its products interoperable with the Design Compiler software. At no point during these cooperative efforts did KBS make any allegation that Synopsys' Design Compiler software, or any other Synopsys product, was infringing the '432 Patent.

63. Aeroflex purchased the Design Compiler software from Synopsys.

64. Plaintiff is barred from recovery of damages by reason of laches.

FOURTH AFFIRMATIVE DEFENSE: IMPLIED LICENSE

65. Plaintiff is barred from obtaining any relief sought in the Am ended Complaint by reason of the existence of an implied license to practice the claims of the '432 Patent between Plaintiff and Synopsys. Plaintiff s action against Aeroflex is barred by the doctrine of patent exhaustion.

FIFTH AFFIRMATIVE DEFENSE: PROSECUTION HISTORY ESTOPPEL

66. By reason of the arguments presented during the prosecution of the applications for the '432 Patent in the United States Patent and Trademark Office, Ricoh is estopped from construing the

claimed inventions of such patent (or any equivalent thereof) as applying to any product made, used, sold, or offered for sale by Aeroflex Incorporated.

SIXTH AFFIRMATIVE DEFENSE: AUTHORIZATION AND CONSENT

67. Ricoh's claims are barred in whole or in part by operation of 28 U.S.C. § 1498.

RESERVATION OF AFFIRMATIVE DEFENSES

68. With discovery still ongoing, Aeroflex has yet to complete its investigation. Aeroflex reserves the right to assert any other defenses that discovery may reveal, including unclean hands or inequitable conduct.

COUNTERCLAIMS

Counterplaintiff Aeroflex, Inc. ("Aeroflex"), for its counterclaims against Counterdefendant Ricoh Company, Ltd. ("Ricoh"), alleges as follows:

PARTIES

69. Aeroflex is a corporation organized under the laws of Delaware, having its principal place of business at 35 S. Service Road, Plainview, NY 11803.

70. Upon information and belief, Ricoh is a corporation organized under the laws of Japan, having its principal place of business at 3 -6 1-chome, Nakamagome, Tokyo, Japan.

JURISDICTION AND VENUE

71. Counts 1 through 2 of the counterclaims are based upon the Patent Laws of the United States, Title 35 of the United States Code, §1 *et seq*. The Court has jurisdiction over the counterclaims pursuant to 28 U.S.C. §§ 1331, 1338(a), 2201, and 2202.

72. Ricoh has submitted to the personal jurisdiction of this Court, because suit was filed in this district by Counterdefendant Ricoh.

73. Venue is proper in this district pursuant to 28 U.S.C. § 1391, because suit was filed in this district by Counterdefendant Ricoh.

74. There is an actual justifiable case or controversy between Aeroflex and Ricoh, in this district, arising under the Patent Laws, 35 U.S.C. § 1 *et seq*. This case or controversy arises by virtue of Ricoh's filing of this suit which purports to allege that Aeroflex infringes U.S. Patent No. 4,922,432

("the '432 Patent") and Aeroflex's Answer thereto, which asserts the invalidity and noninfringement of the '432 Patent.

COUNT 1

DECLARATORY JUDGMENT OF INVALIDITY

75. Aeroflex incorporates by reference Paragraphs 1-74 into this count as though fully set forth herein.

76. The '432 Patent, entitled "Knowledge Based Method and Apparatus for Designing Integrated Circuits using Functional Specifications" issued on May 1, 1990. Ricoh purports to be the owner of the '432 Patent.

77. Ricoh has sued Aeroflex in the present action, alleging infringement of the '432 Patent.

78. Based on Paragraph 58 above, which is specifically incorporated by reference into this Paragraph, the '432 Patent is invalid.

79. Aeroflex requests declaratory judgment that the '432 Patent is invalid.

COUNT 2

DECLARATORY JUDGMENT OF NONINFRINGEMENT

80. Aeroflex incorporates by reference Paragraphs 1-79 into this count as though fully set forth herein.

81. Based on Paragraphs 59 and 60 above, which are specifically incorporated by reference into this Paragraph, the '432 Patent is not infringed by Aeroflex.

82. Aeroflex requests declaratory judgment that Aeroflex has not infringed the '432 Patent.

RESERVATION OF COUNTERCLAIMS

83. Aeroflex reserves the right to assert any other counterclaims that discovery may reveal, including, but not limited to, claims arising out of false or misleading statements to the public and/or customers.

PRAYER FOR RELIEF

WHEREFORE, Aeroflex respectfully prays for the following relief:

A. that this Court deny and all relief requested by Plaintiff in its Amended Complaint and any relief whatsoever, and that the Amended Complaint be dismissed with prejudice;

B. that this Court declare the '432 Patent invalid;

C. that this Court declare the '432 Patent unenforceable;

D. that this Court declare that Aeroflex has not infringed any valid claim of the '432 Patent;

E. that this Court declare the case to be exceptional pursuant to 35 U.S.C. § 285 and that costs of his action and attorneys' fees be awarded to Aeroflex;

F. that this Court grant such other and further relief to Aeroflex as this Court may deem just and equitable and as the Court deems appropriate.

DEMAND FOR JURY TRIAL

Defendant Aeroflex hereby demands trial by jury in this action.

Dated: April 7, 2006

Respectfully submitted,

HOWREY LLP

By: /s/Denise M. De Mory
Denise M. De Mory
Attorneys for Defendants
AEROFLEX, INC., MATROX TECH SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC. AND AEROFLEX COLORADO SPRINGS, INC.

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

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Defendant.

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, et al.,

Defendant.

Case No. C03-04669 MJJ (EMC)

Case No. C03-02289 MJJ (EMC)

NOTICE OF DEPOSITION OF RICOH COMPANY, LTD.PURSUANT TO FED. R. CIV. P. 30(b)(6)

PLEASE TAKE NOTICE that, pursuant to Federal Rule of Civil Procedure 30(b), Defendants AEROFLEX, INC., AMI SEICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD.,

MATROS GRAPHICS, INC. MATROX INTERNATIONAL CORP. and MATROX TECH, INC., by and through its attorneys of record, will take the deposition upon oral examination of the person or persons designated by RICOH COMPANY, LTD. ("Ricoh") as most knowledgeable regarding the subject areas listed below. The deposition will commence on April 25, 2006, or on a date mutually agreed upon by the parties, at 9:00 a.m. at the offices of Howrey LLP, 525 Market Street, Suite 3600, San Francisco, California, and will continue from day to day until completed.

The oral examination may be videotaped and transcribed stenographically, and will take place before an officer who is duly authorized to administer oaths.

Pursuant to Fed. R. Civ. P. 30(b)(6), Ricoh shall produce to testify on its behalf one or more officers, directors, managing agents, or other persons who are most qualified, knowledgeable, and competent to testify as to all matters known or reasonably available to Ricoh with respect to the following topics:

1. Agreements, negotiations, and/or discussions with third parties related to authorizing any use or transfer of the Kobayashi Patent at issue in this litigation, United States Patent Number 4,922,432 ("the Patent"), including but not limited to licensing arrangements and royalties or other compensation related to such arrangements, and including situations in which a license or other transfer was offered by Ricoh but refused or declined by the third party.
2. Royalties or other compensation paid by Ricoh to others for the creation and/or design of ASICs and masks.
3. Ricoh's licensing policies or practices.
4. The value of the Patent.
5. The value of products embodying the technology of the Patent.
6. Litigation, whether threatened or actual, related to the Patent and the results of such litigation or litigation threats, including settlements and/or other compensation.
7. Efforts by Ricoh to obtain public or private funding at any time since filing the application for the Patent.
8. Any and all marketing and sales efforts by Ricoh and/or discussions of market potential that relate in any way to the Patent.
9. Costs to create the Patent.
10. Sales of Ricoh products practicing the Patent.
11. Licenses associated with products practicing the Patent.

12. Sales of other companies' products embodying the Patent.

13. Demand for products practicing the patent and comparisons of such demand versus demand for competing products not using the teachings of the Patent.

14. Non-infringing alternatives for the processes outlined in the Patent.

15. Ricoh's capacity to create the products that Ricoh contends infringe the Patent and were created by Defendants in this litigation.

16. All impacts on Ricoh of the alleged infringement.

17. The commercial success of the Patent or products embodying the Patent.

18. The organizational structure of Ricoh.

19. All damages Ricoh believes it has suffered as a result of the infringement alleged in this litigation, as well as Ricoh's method or methods for accounting for and calculating such damages.

20. Whether Ricoh intends to claim lost profits and if so, the basis of its claim, the amount of profits it believes it lost, and all facts related thereto.

21. Whether Ricoh intends to claim it is entitled to a reasonable royalty and if so, Ricoh's position with respect to each of the fifteen factors for determining a reasonable royalty set forth in *Georgia Pacific Corp. v. United States Plywood Corp.*, 318 F. Supp. 1116, 1120 (S.D.N.Y. 1970), modified and aff'd, 446 F. 2d 295 (2d Cir. 1971).

22. Ricoh's first awareness of products that Ricoh contends satisfy the limitations of the Patent.

23. Ricoh's knowledge, including but not limited to first knowledge, of defendants' alleged infringement of the Patent and all efforts by Ricoh to learn of or investigate the alleged infringement.

Dated: March 2, 2006

HOWREY LLP

By: _____
Denise M. De Mory
Attorneys for Defendants
AEROFLEX, INC., AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC.,

PROOF OF SERVICE

I am employed in the County of San Francisco, State of California. I am over the age of 18 and not a party to the within action. My business address is 525 Market Street, Suite 3600, San Francisco, California 94105.

On _March 2, 2006 I served on the interested parties in said action the within:

NOTICE OF DEPOSITION OF RICOH COMPANY, LTD.PURSUANT TO FED. R. CIV. P. 30(b)(6)

by causing said document to be sent by Electronic Mail on March 2, 2006 to the email addresses indicated for the parties listed below and by placing a true copy thereof in a sealed envelope(s) addressed as stated below and causing such envelope(s) to be delivered as follows:

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I declare under penalty of perjury that I am employed in the office of a member of the bar of this Court at whose direction the service was made and that the foregoing is true and correct.

Executed on March 2, 2006, at San Francisco, California.

Peter L. Kasenenko
(Type or print name)

Peter L. Kasenenko
(Signature)

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Attorneys for Plaintiff SYNOPSYS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendant.	Case No. C-03-2289 MJJ Case No. C-03-4669 MJJ PATENT INFRINGEMENT ACTION **THE CUSTOMER DEFENDANT'S FIRST SET OF REQUESTS FOR ADMISSIONS**
RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, et al., Defendant.	

PROPOUNDING PARTIES: Aeroflex, Inc., Aeroflex Colorado Springs, Inc., AMI Semiconductor Inc., Matrox Graphics, Inc., Matrox Electronics Systems, Ltd. Matrox International Corporation, and Matrox Tech, Inc. ("The Customer Defendants")

RESPONDING PARTY: Defendant Ricoh Company, Ltd.

SET NUMBER: One (1)

The Customer Defendants hereby request that defendant Ricoh Company, Ltd. ("Ricoh") answer the following requests for admission separately, fully, and under oath, pursuant to Rule 36 of

Federal Rules of Civil Procedure, within thirty days of service. Ricoh is required to supplement its responses to these requests in accordance with Federal Rules of Civil Procedure 26(e).

I. DEFINITIONS

A. The terms "Ricoh," "you," and "your" mean, without limitation, Ricoh Company Ltd., its past and present parents, subsidiaries, affiliates, predecessors, unincorporated divisions, officers, attorneys or agents, representatives, employees, consultants and all persons acting or purporting to act on its behalf.

B. The terms "Synopsys" and "Plaintiff" refer, without limitation, to Synopsys, Inc., all subsidiaries, affiliates, predecessors, unincorporated divisions and all its officers, employees, attorneys, agents, representatives and all persons acting or purporting to act on its behalf.

C. The term "Customer Defendants" refers to the defendants in the Ricoh v. Aeroflex et al. case.

D. The term "'432 patent" means United States Patent Number 4,922,432, entitled "Knowledge Based Method and Apparatus For Designing Integrated Circuits Using Functional Specifications."

E. The term "Synopsys products-in-suit" means Design Complier used in conjunction with either VHDL Compiler or HDL Compiler for Verilog.

F. The term "ordinary use" as used herein is a reference to "ordinary use" as described on page 2 in Ricoh's section of the June 8, 2005 Joint Case Management Conference statement.

II. REQUESTS FOR ADMISSION

REQUEST FOR ADMISSION NO. 1:

Admit that on or before January 1, 1995 Ricoh used any version of Synopsys' Design Compiler product that existed on or before January 1, 1995 for logic synthesis of ASICs.

REQUEST FOR ADMISSION NO. 2:

Admit that on or before January 1, 1995 Ricoh used any version of Synopsys' Design Compiler product that existed on or before January 1, 1995 to design ASICs.

REQUEST FOR ADMISSION NO. 3:

Admit that on or before January 1, 1995 Ricoh used any version of Synopsys' HDL Compiler for Verilog product that existed on or before January 1, 1995 for logic synthesis of ASICs.

REQUEST FOR ADMISSION NO. 4:

Admit that on or before January 1, 1995 Ricoh used any version of Synopsys' HDL Compiler for Verilog product that existed on or before January 1, 1995 to design ASICs.

REQUEST FOR ADMISSION NO. 5:

Admit that on or before January 1, 1995 Ricoh used any version of Synopsys' VHDL Compiler product that existed on or before January 1, 1995 for logic synthesis of ASICs.

REQUEST FOR ADMISSION NO. 6:

Admit that on or before January 1, 1995 Ricoh used any version of Synopsys' VHDL Compiler product that existed on or before January 1, 1995 to design ASICs.

REQUEST FOR ADMISSION NO. 7:

Admit that Ricoh was aware on or before January 1, 1997 that Synopsys had licensed any version of Synopsys' Design Compiler product that existed on or before January 1, 1997 to companies other than Ricoh.

REQUEST FOR ADMISSION NO. 8:

Admit that Ricoh was aware on or before January 1, 1997 that Synopsys had licensed any version of Synopsys' HDL Compiler for Verilog product that existed on or before January 1, 1997 to companies other than Ricoh.

REQUEST FOR ADMISSION NO. 9:

Admit that Ricoh was aware on or before January 1, 1997 that Synopsys had licensed any version of Synopsys' VHDL Compiler product that existed on or before January 1, 1997 to companies other than Ricoh.

REQUEST FOR ADMISSION NO. 10:

Admit that Ricoh based its allegations that Matrox Graphics infringes the '432 patent at least in part on information Ricoh obtained from Synopsys as part of Ricoh's licensing relationship with Synopsys.

REQUEST FOR ADMISSION NO. 11:

Admit that Ricoh based its allegations that Matrox Electronic Systems infringes the '432 patent at least in part on information Ricoh obtained from Synopsys as part of Ricoh's licensing relationship with Synopsys.

REQUEST FOR ADMISSION NO. 12:

Admit that Ricoh based its allegations that Matrox Tech infringes the '432 patent at least in part on information Ricoh obtained from Synopsys as part of Ricoh's licensing relationship with Synopsys.

REQUEST FOR ADMISSION NO. 13:

Admit that Ricoh based its allegations that Matrox International infringes the '432 patent at least in part on information Ricoh obtained from Synopsys as part of Ricoh's licensing relationship with Synopsys.

REQUEST FOR ADMISSION NO. 14:

Admit that Ricoh based its allegations that Aeroflex, Inc. infringes the '432 patent at least in part on information Ricoh obtained from Synopsys as part of Ricoh's licensing relationship with Synopsys.

REQUEST FOR ADMISSION NO. 15:

Admit that Ricoh based its allegations that Aeroflex Colorado Springs infringes the '432 patent at least in part on information Ricoh obtained from Synopsys as part of Ricoh's licensing relationship with Synopsys.

REQUEST FOR ADMISSION NO. 16:

Admit that Ricoh has unconditionally agreed not to sue Synopsys for infringement as to any claim of the '432 patent.

REQUEST FOR ADMISSION NO. 17:

Admit that for more than 10 years, Ricoh has been using either VHDL or Verilog as input to any version of the Synopsys products-in-suit.

REQUEST FOR ADMISSION NO. 18:

Admit that for more than 10 years, Ricoh has used register-transfer level descriptions, as described in U.S. Patent No. 4,703,435 at Col. 5:27-34, as input to any version of the Synopsys products-in-suit.

REQUEST FOR ADMISSION NO. 19:

Admit that for more than 10 years, Ricoh has used RTL as input to any version of the Synopsys products-in-suit.

REQUEST FOR ADMISSION NO. 20:

Admit that for more than 10 years, Ricoh has used register-transfer level descriptions, as described in U.S. Patent No. 4,703,435 at Col. 5:27-34, as input to any version of Synopsys' VHDL Compiler product.

REQUEST FOR ADMISSION NO. 21:

Admit that for more than 10 years, Ricoh has used RTL as input to any version of Synopsys' HDL Compiler for Verilog product.

REQUEST FOR ADMISSION NO. 22:

Admit that the inputs for the accused ASICs that the Customer Defendants have produced in this litigation are either VHDL or Verilog.

REQUEST FOR ADMISSION NO. 23:

Admit that the Verilog inputs for the accused ASICs that the Customer Defendants have produced in this litigation are register transfer level descriptions.

REQUEST FOR ADMISSION NO. 24:

Admit that the VHDL inputs for the accused ASICs that the Customer Defendants have produced in this litigation are register transfer level descriptions.

REQUEST FOR ADMISSION NO. 25:

Admit that the Verilog inputs for the accused ASICs that the Customer Defendants have produced in this litigation are register-transfer level descriptions, as described in U.S. Patent No. 4,703,435 at Col. 5:27-34.

REQUEST FOR ADMISSION NO. 26:

Admit that the VHDL inputs for the accused ASICs that the Customer Defendants have produced in this litigation are register-transfer level descriptions, as described in U.S. Patent No. 4,703,435 at Col. 5:27-34.

REQUEST FOR ADMISSION NO. 27:

Admit that generic operators are not examples of synthetic operators.

REQUEST FOR ADMISSION NO. 28:

Admit that HDL arithmetic operators are not "architecture independent actions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 29:

Admit that HDL arithmetic operators are not "architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 30:

Admit that synthetic operators are not "architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 31:

Admit that synthetic modules are not "architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 32:

Admit that generic operators are not "architecture independent actions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 33:

Admit that generic operators are not "architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 34:

Admit that "if" statements are not "architecture independent . . . actions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 35:

Admit that "case" statements are not "architecture independent actions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 36:

Admit that "wait" statements are not "architecture independent actions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 37:

Admit that "always" statements are not "architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 38:

Admit that finite state machines are not "architecture independent actions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 39:

Admit that finite state machines are not "architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 40:

Admit that HDL arithmetic operators are not "definitions of architecture independent actions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 41:

Admit that HDL arithmetic operators are not "architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 42:

Admit that synthetic operators are not "definitions of architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 43:

Admit that synthetic modules are not "definitions of architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 44:

Admit that generic operators are not "definitions of architecture independent actions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 45:

Admit that generic operators are not "definitions of architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 46:

Admit that an "if" statement is not a "definition of an architecture independent action" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 47:

Admit that a "case" statement is not a "definition of an architecture independent action" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 48:

Admit that "wait" statements are not "definitions of architecture independent actions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 49:

Admit that "always" statements are not "definitions of architecture independent . . . conditions" as set forth in Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 50:

Admit that arithmetic operators are not stored in "a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC," as shown on page 13 of the Court's claim construction.

REQUEST FOR ADMISSION NO. 51:

Admit that synthetic operators, such as ADD_UNS_OP, as stored in synthetic libraries, do not constitute "a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC," as shown on page 13 of the Court's claim construction.

REQUEST FOR ADMISSION NO. 52:

Admit that synthetic modules, such as DW01_ADD, as stored in synthetic libraries, do not constitute "a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC," as shown on page 13 of the Court's claim construction.

REQUEST FOR ADMISSION NO. 53:

Admit that placing generic operators, such as MUX_OP, SELECT_OP, DP_OP, SEQGEN, FFGEN, LOGDB, in memory does not constitute storing "a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC," as shown on page 13 of the Court's claim construction.

REQUEST FOR ADMISSION NO. 54:

Admit that creating an implementation table in computer memory does not constitute storing "a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC," as shown on page 13 of the Court's claim construction.

REQUEST FOR ADMISSION NO. 55:

Admit that in V-2003.12-SP1, actions and conditions are never stored together in "a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC," as shown on page 13 of the Court's claim construction.

REQUEST FOR ADMISSION NO. 56:

Admit that the "library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC" identified in Ricoh's Final Infringement Contentions does not exist in its entirety prior to a design being read into the Design Compiler System.

REQUEST FOR ADMISSION NO. 57:

Admit that both actions and conditions must be contained in a single library to constitute "a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC," as shown on page 13 of the Court's claim construction.

REQUEST FOR ADMISSION NO. 58:

Admit that the implementation table, in any version of the Synopsys products-in-suit, is created only after a design is read into the Design Compiler System.

REQUEST FOR ADMISSION NO. 59:

Admit that the generic operators, in any version of the Synopsys products-in-suit, are loaded into memory only when the Design Compiler System is executed.

REQUEST FOR ADMISSION NO. 60:

Admit that in Claim 13 of U.S. Patent 4,922,432 "a set of definitions of architecture independent actions and conditions" must be stored prior to "describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions."

REQUEST FOR ADMISSION NO. 61:

Admit that in Claim 13 of U.S. Patent 4,922,432 "a set of definitions of architecture independent actions and conditions" must be stored prior to "specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed."

REQUEST FOR ADMISSION NO. 62:

Admit that in Claim 13 of U.S. Patent 4,922,432 the "a set of definitions of architecture independent actions and conditions" must be stored prior to "selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base."

REQUEST FOR ADMISSION NO. 63:

Admit that a "rule," as described in claim 13 of U.S. Patent No. 4,922,432 must include both an antecedent portion and a consequent portion.

REQUEST FOR ADMISSION NO. 64:

Admit that you claim that any IF-THEN statement is "rule" as defined in the Court's April 7, 2006 Claim Construction Order.

REQUEST FOR ADMISSION NO. 65:

Admit that if the consequent portion of one or more rules is not applied to a design during logic synthesis, then there has been "selective application" of the rules.

REQUEST FOR ADMISSION NO. 66:

Admit that if the "THEN" portion of one or more rules is not applied to a design during logic synthesis, then there has been "selective application" of the rules.

REQUEST FOR ADMISSION NO. 67:

Admit that if the antecedent portions of every rule in an expert system knowledge base is tested during logic synthesis of an ASIC design, then there is not "selective application" of the rules.

REQUEST FOR ADMISSION NO. 68:

Admit that the antecedent portion of every "SOT trick" is tested or "tried" during logic synthesis of an ASIC design.

REQUEST FOR ADMISSION NO. 69:

Admit that the antecedent portion of every "SDN trick" is tested or "tried" during logic synthesis of an ASIC design.

REQUEST FOR ADMISSION NO. 70:

Admit that every "SOT trick" and "SDN trick" is attempted during logic synthesis of an ASIC design.

REQUEST FOR ADMISSION NO. 71:

Admit that if the "IF" condition of every SOT trick is tested during logic synthesis, then the SOT tricks are not selectively applied.

REQUEST FOR ADMISSION NO. 72:

Admit that if the "IF" condition of every SDN trick is tested during logic synthesis, then the SDN tricks are not selectively applied.

REQUEST FOR ADMISSION NO. 73:

Admit that if the "IF" condition of every SOT and SDN trick is tested during logic synthesis, then the SOT and SDN tricks are not selectively applied.

REQUEST FOR ADMISSION NO. 74:

Admit that Ricoh claims that the "expert knowledge of highly skilled VLSI designers," as shown on page 17 of the claim construction order, embodied in the Design Compiler System originated in the Socrates system.

REQUEST FOR ADMISSION NO. 75:

Admit that the Socrates system predated the filing of the patent application that became U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 76:

Admit that Ricoh cannot identify any "rules" in the Socrates system that continue to be used in the Design Compiler System.

REQUEST FOR ADMISSION NO. 77:

Admit that if "architecture independent actions and conditions" are explicitly included in the input specification for the design of an ASIC, they are not "described," as that term is defined on page 13 of the claim construction order.

REQUEST FOR ADMISSION NO. 78:

Admit that if arithmetic operators are explicitly included in the input specification for the design of an ASIC, they are not "described," as that term is defined on page 13 of the claim construction order.

REQUEST FOR ADMISSION NO. 79:

Admit that if "if" statements are explicitly included in the input specification for the design of an ASIC, they are not "described," as that term is defined in the Court's April 7, 2005 Claim Construction Order.

REQUEST FOR ADMISSION NO. 80:

Admit that if "case" statements are explicitly included in the input specification for the design of an ASIC, they are not "described," as that term is defined in the Court's April 7, 2005 Claim Construction Order.

REQUEST FOR ADMISSION NO. 81:

Admit that if "wait" statements are explicitly included in the input specification for the design of an ASIC, they are not "described," as that term is defined in the Court's April 7, 2005 Claim Construction Order.

REQUEST FOR ADMISSION NO. 82:

Admit that if "always" statements are explicitly included in the input specification for the design of an ASIC, they are not "described," as that term is defined in the Court's April 7, 2005 Claim Construction Order.

REQUEST FOR ADMISSION NO. 83:

Admit that the HDL Compilers commands "analyze" and "elaborate" must be used to satisfy the step of "specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed" of Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 84:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to arithmetic operators.

REQUEST FOR ADMISSION NO. 85:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to synthetic operators.

REQUEST FOR ADMISSION NO. 86:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to synthetic modules.

REQUEST FOR ADMISSION NO. 87:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to generic operators.

REQUEST FOR ADMISSION NO. 88:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to "if" statements.

REQUEST FOR ADMISSION NO. 89:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to "case" statements.

REQUEST FOR ADMISSION NO. 90:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to "wait" statements.

REQUEST FOR ADMISSION NO. 91:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to "always" statements.

REQUEST FOR ADMISSION NO. 92:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to finite state machines.

REQUEST FOR ADMISSION NO. 93:

Admit that "SOT tricks" and "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are only applied to cells that have already been mapped to a technology library.

REQUEST FOR ADMISSION NO. 94:

Admit that neither "SOT tricks" nor "SDN tricks" in the V-2003.12-SP1 version of Design Compiler are applied to the input HDL description.

REQUEST FOR ADMISSION NO. 95:

Admit that a netlist output from Design Compiler must contain all of "the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor" to meet the last element of Claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 96:

Admit that netlist output from Design Compiler which does not contain all of "the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor" does not satisfy the last element from claim 13 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 97:

Admit that the netlist output from Design Compiler for a mixed signal ASIC would only include hardware cells for the digital portions of the ASIC.

REQUEST FOR ADMISSION NO. 98:

Admit that the netlist output from Design Compiler is changed in the place and route process.

REQUEST FOR ADMISSION NO. 99:

Admit that the netlist output from Design Compiler is not directly used to generate GDSII files.

REQUEST FOR ADMISSION NO. 100:

Admit that the netlist output from the place and route process is directly used to generate GDSII files.

REQUEST FOR ADMISSION NO. 101:

Admit that you do not claim that any Customer Defendant's use of the Design Compiler System is anything but "ordinary use."

REQUEST FOR ADMISSION NO. 102:

Admit that Ricoh does not have any basis for claiming that Aeroflex Incorporated makes, uses, imports, sell, or offers to sell within the United States or exports from the United States ASICs made by the process recited in claims 13-17 of U.S. Patent No. 4,922,432.

REQUEST FOR ADMISSION NO. 103:

Admit that if a VHDL design containing only the statements "if csy or counter = 63 then counter <= 0; else" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, no output will result.

REQUEST FOR ADMISSION NO. 104:

Admit that if a VHDL design containing only the statements "if csy or counter = 63 then counter <= 0; else" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, a syntax error will result.

REQUEST FOR ADMISSION NO. 105:

Admit that if a VHDL design containing only the statements "if csy or counter = 63 then counter <= 0; else" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not constitute a netlist for an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 106:

Admit that if a VHDL design containing only the statements "if csy or counter = 63 then counter <= 0; else" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not define the hardware cells and interconnections necessary to fabricate an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 107:

Admit that if a VHDL design containing only the statements "begin pe_az_data_sum <= pe_az_data_signed + pe_az_sum_out; end process;" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, no output will result.

REQUEST FOR ADMISSION NO. 108:

Admit that if a VHDL design containing only the statements "begin pe_az_data_sum <= pe_az_data_signed + pe_az_sum_out; end process;" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, a syntax error will result.

REQUEST FOR ADMISSION NO. 109:

Admit that if a VHDL design containing only the statements "begin pe_az_data_sum <= pe_az_data_signed + pe_az_sum_out; end process;" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not constitute a netlist for an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 110:

Admit that if a VHDL design containing only the statements "begin pe_az_data_sum <= pe_az_data_signed + pe_az_sum_out; end process;" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not define the hardware cells and interconnections necessary to fabricate an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 111:

Admit that if a VHDL design containing only the statements "v_ramp_down_res target := new_position + RAMP_DOWN_START; -- 168=159+(3*3Freqs) pos_state <= move 0;" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, no output will result.

REQUEST FOR ADMISSION NO. 112:

Admit that if a VHDL design containing only the statements "v_ramp_down_res target := new_position + RAMP_DOWN_START; -- 168=159+(3*3Freqs) pos_state <= move 0;" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, a syntax error will result.

REQUEST FOR ADMISSION NO. 113:

Admit that if a VHDL design containing only the statements "v_ramp_down_res target := new_position + RAMP_DOWN_START; -- 168=159+(3*3Freqs) pos_state <= move 0;" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not constitute a netlist for an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 114:

Admit that if a VHDL design containing only the statements "v_ramp_down_res target := new_position + RAMP_DOWN_START; -- 168=159+(3*3Freqs) pos_state <= move 0;" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not define the hardware cells and interconnections necessary to fabricate an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 115:

Admit that if a Verilog design containing only the statements "always @(posedge clock or posedge rst) if (rst) hold <= 0; else" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, no output will result.

REQUEST FOR ADMISSION NO. 116:

Admit that if a Verilog design containing only the statements "always @(posedge clock or posedge rst) if (rst) hold <= 0; else" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, a syntax error will result.

REQUEST FOR ADMISSION NO. 117:

Admit that if a Verilog design containing only the statements "always @(posedge clock or posedge rst) if (rst) hold <= 0; else" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not constitute a netlist for an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 118:

Admit that if a Verilog design containing only the statements "always @(posedge clock or posedge rst) if (rst) hold <= 0; else" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not define the hardware cells and interconnections necessary to fabricate an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 119:

Admit that if a Verilog design containing only the statements "else begin case (sample_num) 0: accum <= accum + sample[0];" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, no output will result.

REQUEST FOR ADMISSION NO. 120:

Admit that if a Verilog design containing only the statements "else begin case (sample_num) 0: accum <= accum + sample[0];" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, a syntax error will result.

REQUEST FOR ADMISSION NO. 121:

Admit that if a Verilog design containing only the statements "else begin case (sample_num) 0: accum <= accum + sample[0];" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not constitute a netlist for an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 122:

Admit that if a Verilog design containing only the statements "else begin case (sample_num) 0: accum <= accum + sample[0];" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not define the hardware cells and interconnections necessary to fabricate an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 123:

Admit that if a VHDL design containing only the statements "case astate is when IDO => if (apostate ='1') then" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, no output will result.

REQUEST FOR ADMISSION NO. 124:

Admit that if a VHDL design containing only the statements "case astate is when IDO => if (apostate ='1') then" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, a syntax error will result.

REQUEST FOR ADMISSION NO. 125:

Admit that if a VHDL design containing only the statements "case astate is when IDO => if (apostate ='1') then" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not constitute a netlist for an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 126:

Admit that if a VHDL design containing only the statements "case astate is when IDO => if (apostate ='1') then" is input into the V-2003.12-SP1 version of the Synopsys products-in-suit, the resulting netlist does not define the hardware cells and interconnections necessary to fabricate an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 127:

Admit that mask data cannot be used directly to fabricate an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 128:

Admit that mask data is used to create a mask prior to the fabrication of an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 129:

Admit that the rules identified in Col. 11:48-12:29 of the '432 patent are exemplary only.

REQUEST FOR ADMISSION NO. 130:

Admit that the rules identified in Col. 11:48-12:29 of the '432 patent are exemplary only and are not intended to be a complete set of rules for a expert system knowledge base.

REQUEST FOR ADMISSION NO. 131:

Admit that the rules identified in Col. 11:48-12:29 of the '432 patent are not intended to be a complete set of rules for an "expert system knowledge base" as used in Claim 13 of the '432 patent.

REQUEST FOR ADMISSION NO. 132:

Admit that the rules identified in Col. 11:48-12:29 of the '432 patent are a complete set of rules for an "expert system knowledge base" as used in Claim 13 of the '432 patent.

REQUEST FOR ADMISSION NO. 133:

Admit that an application specific integrated circuit design tool that included only the rules set forth in Col. 11:48-12:29 of the '432 patent could not be used to create a netlist for an application specific integrated circuit.

REQUEST FOR ADMISSION NO. 134:

Admit that in 1988 the KBSC system had more rules than are disclosed in the '432 patent.

REQUEST FOR ADMISSION NO. 135:

Admit that in 1989 the KBSC system had more rules than are disclosed in the '432 patent.

REQUEST FOR ADMISSION NO. 136:

Admit that in 1990 the KBSC system had more rules than are disclosed in the '432 patent.

REQUEST FOR ADMISSION NO. 137:

Admit that mapping HDL operators to synthetic operators, in the V-2003.12-SP1 version of the Synopsys products-in-suit, does not include applying "rules" as the term "rules" is used in Claim 13 of the '432 patent.

REQUEST FOR ADMISSION NO. 138:

Admit that mapping HDL operators to synthetic operators, in the V-2003.12-SP1 version of the Synopsys products-in-suit, does not include applying "cell selection rules" as the term "cell selection rules" is used in Claim 13 of the '432 patent.

REQUEST FOR ADMISSION NO. 139:

Admit that mapping synthetic operators to synthetic modules, in the V-2003.12-SP1 version of the Synopsys products-in-suit, does not include applying "rules" as the term "rules" is used in Claim 13 of the '432 patent.

REQUEST FOR ADMISSION NO. 140:

Admit that mapping synthetic operators to synthetic modules, in the V-2003.12-SP1 version of the Synopsys products-in-suit, does not include applying "cell selection rules" as the term "cell selection rules" is used in Claim 13 of the '432 patent.

REQUEST FOR ADMISSION NO. 141:

Admit that mapping generic operators to synthetic modules, in the V-2003.12-SP1 version of the Synopsys products-in-suit, does not include applying "rules" as the term "rules" is used in Claim 13 of the '432 patent.

REQUEST FOR ADMISSION NO. 142:

Admit that mapping generic operators to synthetic modules, in the V-2003.12-SP1 version of the Synopsys products-in-suit, does not include applying "cell selection rules" as the term "cell selection rules" is used in Claim 13 of the '432 patent.

REQUEST FOR ADMISSION NO. 143:

Admit that mapping synthetic modules to DesignWare implementations, in the V-2003.12-SP1 version of the Synopsys products-in-suit, does not include applying "rules" as the term "rules" is used in Claim 13 of the '432 patent.

REQUEST FOR ADMISSION NO. 144:

Admit that mapping synthetic modules to DesignWare implementations, in the V-2003.12-SP1 version of the Synopsys products-in-suit, does not include applying "cell selection rules" as the term "cell selection rules" is used in Claim 13 of the '432 patent.

Dated: April 17, 2006

HOWREY LLP

By: _____
Ethan B. Andelman
Attorneys for Plaintiff Synopsys, Inc.

PROOF OF SERVICE

STATE OF CALIFORNIA)
) ss.:
COUNTY OF SAN FRANCISCO)

I am employed in the County of San Francisco, State of California. I am over the age of 18 and not a party to the within action. My business address is 525 Market Street, Suite 3600, San Francisco, California 94105.

On April 17, 2006 I served on the interested parties in said action the within:

THE CUSTOMER DEFENDANT'S FIRST SET OF REQUESTS FOR ADMISSIONS

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I declare under penalty of perjury that I am employed in the office of a member of the bar of this Court at whose direction the service was made and that the foregoing is true and correct.

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Patricia Cranmer
(Type or print name)

Patricia Cranmer
(Signature)

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Avant! Shakes Up Front-End Design - Jupiter CAE software - Product Announcement

Ann Steffora

Scottsdale, Ariz.-Avant! Corp., Fremont, Calif., last week charged into the great submicron land grab with the announcement of Jupiter, a new product that the company is billing as a complete front-end design creation tool.

With the announcement, Avant! becomes just the latest EDA vendor to cater to OEMs' need to retool for deep submicron designs. The lead up to this week's 36th Annual Design Automation Conference in New Orleans has seen a number of companies introduce tools that consider the physical effects of design decisions early in the planning stage to reduce cycle times. The companies are hoping these capabilities will lure business away from competitors during the submicron transition.

Avant!'s Jupiter is positioned to compete directly with the Chip Architect product from Mountain View, Calif.,-based Synopsys Inc. As its foundation, Chip Architect uses Physical Synthesis, which is the incorporation of physical data in the early design planning stages for early timing prediction. Cadence Design Systems Inc., San Jose, also is said to be preparing its approach to deep-submicron, high-level design planning.

Avant! said its approach to the front end is different from the competition because, as in its other deep-submicron design tools, the company's Milkyway database serves as the backbone for Jupiter. The use of Milkyway eliminates the need for complex interfaces between tools, Avant! said.

Jupiter also contains a synthesis capability, which has spurred speculation that Jupiter could pose a challenge to Synopsys' Design Compiler tool. However, Avant! is not immediately planning to market Jupiter as a Design Compiler replacement, said Michael Jackson, head of product management for Avant!.

Synopsys' Design Compiler still leads the synthesis market with 81 percent market share in 1997, according to the market research firm Dataquest, San Jose. Even if Avant!'s technology proves to be as formidable as it asserts, unseating Synopsys may not likely occur for a number of years.

Although not the immediate plans, observers believe this is the direction Avant! will take, since best results are obtained by using the integrated synthesizer in Jupiter. The real question is whether OEMs will buy into the strategy.

Industry experts are not so excited about Avant!'s stance.

"The message is that, of course you can use Design Compiler, but it won't work as well," said Gary Smith, chief analyst of worldwide EDA at Dataquest. "Probably more important is how many engineers will drop their Cadence or Synopsys simulator. Design libraries are really tied to your simulator. To use Jupiter, the RTL tool flow has to be changed completely and there's not a lot of chance that will happen."

While a silicon vendor will adopt anything in order to get more (and bigger) designs in the door, unfortunately, unlike the IC CAD world, engineers buy CAE tools. And selling CAE tools is a whole different world than selling CAD tools, Smith said. Therein lies Avant!'s main barrier to success with Jupiter, he said.

Changing an entire tool flow is a daunting task for any OEM. Thus some OEMs may choose to use more open EDA tools for the

flexibility of tool choices, in order to leverage existing knowledge and protect productivity of design teams.

Soccol, Jason

From: Soccol, Jason
Sent: Friday, May 26, 2006 4:19 PM
To: Soccol, Jason; 'brothersk@dsmo.com'; 'hoffmang@dsmo.com'; 'meilmane@dsmo.com'; 'olivere@dsmo.com'; 'allend@dsmo.com'; 'weinsteinm@dsmo.com'
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Attachments: 05_26_06_Soccol_Ltr_Brothers_Re_Production.pdf

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Counsel:

Please see the attached production letter with Federal Express tracking slip.

Should you have any questions or comments, please do not hesitate to contact me.

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VIA FEDERAL EXPRESS OVERNIGHT

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DICKSTEIN, SHAPIRO, MORIN & OSHINSKY, LLP
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Exhibit 15

Title: Design Automation Assistant – CMU

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[Kowalski 85d] Kowalski, Geiger, Wolf, Fichtner "The VLSI Design Automation Assistant: A Birth in Industry" 1985 ISCAS 889-892 (1985), DEF 018660 - 018664.

[Kowalski88] Kowalski, "The VLSI Design Automation Assistant: An Architecture Compiler," Silicon Compilation ch. 5 (ed. Gajski) (1988). (edited reprint of Kowalski85b), DEF 006791 - 006821.

storing a set of definitions of architecture independent actions and conditions;	A compiler, a program stored and executed on a computer, stores predefined operators that are used in preparing a dataflow graph representation from an ISPS source file. *See* [Kowalski85c] at 36. "The ISPS language ... can now be used to describe the functional behavior of any digital system." [Director81] at 637. "The ISPS description is considered an algorithmic description, not a representation of the structure of the implementation." [Kowalski85c] at 47. "The key parameter that permits the realization of such an exploration of alternative designs is the fact that the initial behavioral description does not specify the actual implementation. By not specifying the actual components, the system is free to try alternative realizations, evaluate them, and select the best one." [Barbacci81] at 35. "ISPS describes ... the behavior of the hardware units ... The behavioral aspects of the unit are described by procedures which specify the sequence of control and data operations in the machine." [Barbacci81] at 25. "ISPS allows the declaration of procedures, which contain ... data and control operations." [Barbacci81] at 26. "An ISPS description consists of a series of declaration of entities. Some of these are simple carriers, which hold the data being manipulated, similar to variables in a programming language. Other entities are procedures of functions much like the procedures or functions of a programming language. These define how the data is manipulated. The procedures are specified by data operators that do arithmetic, logical, relational, and shift operations on the data [i.e. actions], and by sequential, parallel, and conditional constructs that show the data operators are combined [i.e. conditions]." [Kowalski85b] at 46-47. "The DAA actually works from a dataflow representation extracted from the ISPS description." [Kowalski85c] at 36.

	CMU DAA is a computer-aided design system for designing an ASIC from functional specifications. Figure 1 of Kowalski85c illustrates a multi-stage process that uses a computer to assist in the design of a special purpose VLSI chip. [Kowalski85c] at 34. The process employs at least one computer aided design

storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;	There are two such databases taught by Kowalski85c that collectively or individually meet this limitation. First, there is the database used by the DAA that stores data describing a set of technology sensitive modules, *see* [Kowalski85c] at 35, which are hardware cells under the broadest reasonable interpretation. "The DAA uses a technology-sensitive database… The technology-sensitive database contains expert knowledge about the trade-offs particular to the target technology;" [Kowalski85c] at 34-35. "This technique allows easy change of target technologies and the individual fine tuning of design constraints." [Kowalski85b] at 39. Second, there is the database used by the module binder that stores data describing a set of available integrated hardware cells. *See* [Kowalski85c] at 37. "The module binder chooses physically realizable technology-dependent cells to implement the technology-independent modules in the DAA's design. The cells are chosen from the module database on the basis of user-supplied constraints on functionality, power dissipation, delay, and area." [Kowalski85d] at 891. "MOBY employs a standard cell approach to binding hardware to the modules of the data path. Interchangeable cell libraries which were provided by industrial affiliate are used. The cell libraries in use contain gate array cells, however MOBY was designed to be used with any standard cell library. The standard cell approach is appropriate for a module binder for the CMU-DA system." [Dirkes85] at 6. "The technology-dependent modules are either selected from the module database or fabricated from simpler, equivalent database entries." [Kowalski85c] at 35.
storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;	"A cornerstone of our hardware synthesis approach is the use of knowledge-based expert systems. Such systems make decisions based on knowledge, expressed as rules, obtained from expert designers." [Kowalski85c] at 34. For example, the DAA, a knowledge-based expert system, stores a set of rules for selecting technology sensitive modules that perform each of the specified actions or conditions, wherein each rule embodies the knowledge of expert VLSI chip designers and is stored in an expert system knowledge base. *See* [Kowalski85c] at 36. Through application of these rules, the DAA maps the architectural independent actions or conditions into technology sensitive modules, linking paths and control logic, and then it optimizes the resulting design. *See* [Kowalski85c] at 34. "The DAA is implemented as a production system using the OPS5

	knowledge-based expert-system, KBES, writing system." [Kowalski85a] at 252. "The rule memory is a collection of conditional statements that operate on elements stored in the working memory." [Kowalski85b] at 28. "The prototype DAA system had about 70 rules… The development DAA system now has over 300 rules and has designed a much better MCS6502 microcomputer." [Kowalski85b] at 29. "Rules were added to recognize when a multiplexer should be converted to a bus and how to share that bus with other distributed multiplexers." [Kowalski85b] at 34. *See also* chapter 5 [Kowalski85b] at 62-97 and Table 14.
describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions;	"[T]he design process begins with a behavioral specification of the digital system to be designed. Such a specification provides a model which accurately characterizes the input-output behavior of the system without reflecting any internal structure. This level of specification might be expressed in terms of a flowchart, or as we choose to do below, in terms of a high-level hardware description language." [Director82] at 635. "Inputs to the system will be a behavioral description of the hardware to be designed, objectives which specify the user's optimization criteria, and a library specifying the components available to the design system." [Hafer82] at 93, 2nd col. This element is met by Kowalski85c when the ISPS source file is entered by a user. The ISPS source file is an algorithmic description of the functionality of the desired chip written by the designer that is not tied to any particular implementation style, fabrication technology, or structure. *See* [Kowalski85c] at 34. "The designer first specifies the chip's functionality as an algorithm. The algorithmic description is not tied to a particular implementation style [architecture], such as parallel or serial, sequential or pipelined." [Kowalski85c] at 34. "The DAA is a knowledge-based expert system that uses a database of over 500 rules to synthesize an architectural implementation from an algorithmic description with constraints. The description is written in ISPS" [Kowalski85c] at 36. "The DAA actually works from a dataflow representation extracted from the ISPS description." [Kowalski85c] at 36. "The ISPS language … can now be used to describe the functional behavior of any digital system" [Director81] at 637. "An ISPS description consists of a series of declarations of entities. Some of these are simple carriers, which hold the data being manipulated,

	similar to variables in a programming language. Other entities are procedures or functions much like the procedures or functions of a programming language. These define how the data is manipulated. The procedures are specified by data operators that do arithmetic, logical, relational, and shift operations on the data [i.e. actions] and by sequential, parallel, and conditional constructs that show how the data operators are combined [i.e. conditions]." [Kowalski85b] at 46-47. "The ISPS description is considered an algorithmic description, not a representation of the structure of the implementation. [i.e. architecture independent]" [Kowalski85b] at 47. "The key parameter that permits the realization of such an exploration of alternative designs is the fact that the initial behavioral description does not specify the actual implementation. By not specifying the actual components, the system is free to try alternative realizations, evaluate them, and select the best one." [Barbacci81] at 35. "ISPS describes … the behavior of the hardware units… The behavioral aspects of the unit are described by procedures which specify the sequence of control and data operations in the machine". [Barbacci81] at 25. "ISPS allows the declaration of procedures, which contain … data and control operations" [Barbacci81] at 26. See, e.g., Figure 3 in [Director82] at 637 for an example design of a PDP-8 computer.
specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and	"The DAA actually works from a dataflow representation extracted from the ISPS description." [Kowalski85c] at 36. "An ISPS description consists of a series of declarations of entities. Some of these are simple carriers, which hold the data being manipulated, similar to variables in a programming language. Other entities are procedures or functions much like the procedures or functions of a programming language. These define how the data is manipulated. The procedures are specified by data operators that do arithmetic, logical, relational, and shift operations on the data [i.e. actions] and by sequential, parallel, and conditional constructs that show how the data operators are combined [i.e. conditions]." [Kowalski85b] at 46-47. "The ISPS description is considered an algorithmic description, not a representation of the structure of the implementation. [i.e. architecture independent]" [Kowalski85b] at 47. "The ISPS description is compiled into a VT data-flow representation… . The VT is a directed acyclic graph, DAG, similar in nature to those used in optimizing compilers, with the addition of control constructs to allow conditionals and subroutines in the VT. The nodes in the graph are called operators and correspond to operations that take certain values as input and produce new values as output. They are translations of the ISPS unary and binary operations [i.e. actions], operations that change or access fields

	in words or words in arrays, control operations such as procedure or block invocation, and conditional branches. [i.e. conditions]" [Kowalski85b] at 49. "The main characteristic [of the ISPS paradigm] is the use of a formally defined intermediate representation for the parse trees. This intermediate format (called Global Data Base or GDB, for short) can be easily used by a multitude of application programs, written in any language and running on any machine." [Barbacci81] at 25. In Fig. 1 on page 25, it is clear that the ISPS description is run through the parser to get to the GDB. "The ISP description is transformed into an alternative representation called the ValueTrace or VT" [Director82] at 638, col. 2. See, e.g., Figure 3 in [Director82] at 637 for an example design of a PDP-8 computer.
selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit	"A cornerstone of our hardware synthesis approach is the use of knowledge-based expert systems. Such systems make decisions based on knowledge, expressed as rules, obtained from expert designers." [Kowalski85c] at 34. "The initial knowledge in the system was codified from the algorithms of the current CMU/DA allocator and the interviews [with chip design experts] discussed above." [Kowalski85b] at 26. "The DAA is implemented as a production system using the OPS5 knowledge-based expert-system, KBES, writing system." [Kowalski85a] at 252. "[DAA] begins by allocating the base variable storage elements … to hardware modules and ports. Next, it maps all data-flow operator outputs not bound to base-variable storage elements to register modules. Last, it maps each data-flow operator, with its inputs and outputs to modules, ports, and links." "The prototype DAA system had about 70 rules… The development DAA system now has over 300 rules and has designed a much better MCS6502 microcomputer." [Kowalski85b] at 29. "Rules were added to recognize when a multiplexer should be converted to a bus and how to share that bus with other distributed multiplexers." [Kowalski85b] at 34. "The DAA is a knowledge-based expert system that uses a database of over 500 rules to synthesize an architectural implementation from an algorithmic description with constraints. The description is written in ISPS". [Kowalski85c] at 36. "The knowledge-based expert system approach followed by the DAA uses a weak method, match [an inference engine methodology], in place of

hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

extensive backtracking." [Kowalski85c] at 36.

"The number of rule firings, or activations, for the complete design of the structured control-flow processor, SCF3, is provided in Table 1." [Kowalski85a] at 252-253.

Table 1. RULES BY FUNCTION

Section	Rules	Firings
Service Functions	88	4901
Global Allocation	78	104
Dataflow Allocation	55	1468
Module Allocation	47	1610
Global Improvements	46	460
Total DAA	314	8543

See discussion regarding the rules in Table 1. [Kowalski85a] at 253-254. *See also* chapter 5 [Kowalski85b] at 62-97.

"Primarily there are two estimators. One bridges the algorithmic to fabrication-dependent hardware-network level as a partitioner, while the other bridges the technology-independent to the technology-dependent hardware-network level as a cost function." [Kowalski85b] at 84.

"[Various factors] must be quantified, weighted, and combined to give a measure of how expensive a new module would be as opposed to the cost of sharing an already existing module." [Kowalski85b] at 88.

"This rule shows an important use of the technology database as part of the rule." [Kowalski85b] at 37.

"Rules that manage the technology-independent database." [Kowalski85b] at 39.

"The next type of management is module management. This set of rules has knowledge about creating, combining, and removing modules from the design. These rules allow the designer and thus the other rules in the DAA, to think about creating, combining and removing modules as atomic units, rather than as individual parts. [Kowalski85b] at 65.

"The decision making connected with the results of these estimators was kept in rules, but the calculation was moved to a C program... Primarily there are two estimators. One bridges the algorithmic to fabrication-dependent level as a partitioner, while the other bridges the technology-independent to the technology-dependent hardware-network level as a cost

	function." [Kowalski85b] at 83-84. "The module binder chooses physically realizable technology-dependent cells to implement the technology-independent modules in the DAA's design. The cells are chosen from the module database on the basis of user-supplied constraints on functionality, power dissipation, delay, and area." [Kowalski85d] at 891. "The module binder selects physical modules from the module set library to implement the generic components in the data path." [Hafer82] at 94, 2nd col. "The control allocator translates the technology-independent control specification, generated by the DAA, into a controller implementation in a chosen technology." [Kowalski85c] at 37. "The Design Automation Assistant is a knowledge-based expert-system, KBES, that generates a technology-independent list of operators, registers, data paths and control signals from an algorithmic description of a VLSI system." [Kowalski85a] at 252 See also [Kowalski83b] at 186 and [Kowalski83a] at 479. "The DAA produces a technology-independent hardware network description. This description is composed of modules [i.e. cells], ports, links [i.e. interconnection requirements], and a symbolic microcode. The modules can be registers, operators, memories, and buses or multiplexers with input, output, and bidirectional ports. The ports are connected by links and are controlled by symbolic microcode." [Kowalski85b] at 26. "The technology-independent, but technology-sensitive implementation description is given in a structure and control specification language, SCS (soon to be replaced by DIF). The structural specification models the functional and logical structural levels as a network of modules." [Kowalski85b] at 51-52. "The floor planner produces an abstract physical design for the technology-dependent network designed by the DAA and the module binder." [Kowalski85c] at 37. "Figure 4. Sample netlist to floor plan transformation." [Kowalski85c] at 37. The DAA, a knowledge-based expert system, first selects, for each of the architecture independent actions and conditions of the algorithmic description, one or more technology sensitive modules. *See* [Kowalski85c] at 35. The module binder then binds each of these modules to an integrated circuit hardware cell. [Kowalski85c] at 37.
14. A process as defined in claim 13, including generating from the	"The VLSI Design Automation Assistant: From Algorithms to Silicon." [Kowalski85c] at 33. "A series of programs translates an algorithm into a chip design."

netlist the mask data required to produce an integrated circuit having the desired function.	[Kowalski85c] at 33. *See* Figure 1 of [Kowalski85c] at 34. "The floor planner produces an abstract physical design for the technology-dependent network [a.k.a. netlist] designed by the DAA and the module binder." [Kowalski85c] at 37. "The data-path floor planner (DP): a knowledge-based expert system that is responsible for the complete physical design of the chip. It arranges the modules selected by the module binder and control allocator into a data-path floor plan and creates the cell-layout parameters". [Kowalski85c] at 35. "At the same time the floor plan is being built, the specifications for the modules – size, shape, delay, etc. – are being refined. These specifications will be passed to the module generators to guide the production of the cells." [Kowalski85c] at 38. "The generator program produces a Lava description of a cell from parameters that define the requirements on the cell." [Kowalski85c] at 39. "The Lava chip compiler compacts the individual cells and assembles them into a chip according to the floor plan… This symbolic layout can be macro-expanded into a pure layout that can be used to fabricate the chip." [Kowalski85c] at 40. "The symbolic layout can be can be made into masks to manufacture the integrated circuit." [Kowalski85d] at 890. "The netlist can be used as input to any existing VLSI layout and routing tool 16 to create mask data 18 for geometrical layout." '432 patent, 4:44-46. "Computer-aided design systems for cell placement and routing are commercially available which will lay out the respective cells in the chip, generate the necessary routing, and produce mask data which can be directly used by a chip foundry in the fabrication of integrated circuits." *Id.* at 5:40-46. "From this netlist the mask data for producing the integrated circuit can be directly produced using available VLSI CAD tools." *Id.* at 14:4-7.
15. A process as defined in claim 13 including the further step of generating data paths for the selected integrated circuit hardware	"The Design Automation Assistant is a knowledge-based expert-system, KBES, that generates a technology-independent list of operators, registers, data paths and control signals from an algorithmic description of a VLSI system." [Kowalski85a] at 252 See also [Kowalski83b] at 186 and [Kowalski83a] at 479. "DAA synthesizes a technology-independent representation of memories, registers, operators, data-paths and timing signals from an algorithmic description of a VLSI system." [Kowalski85b] at 46.

cells.	"Our approach seeks to aid the designer with tools that automatically produce data paths and control sequences from an algorithmic system description within user-specified constraints". [Kowalski85c] at 33. "The DAA allocates the clock phases, operators, registers, data paths and control logic in two subtasks, dataflow allocation and module allocation, which are shown in Figure 1. This allows the DAA to gather all the information about register usage in the dataflow allocation and then allocate registers and modules in the module allocation." [Kowalski85a] at 253. "The data-path floor planner (DP): a knowledge-based expert system that is responsible for the complete physical design of the chip. IT arranges the modules selected by the module binder and control allocator into a data-path floor plan and creates the cell-layout parameters." [Kowalski85c] at 35. "Synthesis of the data path is separated into two steps:..." [Director 82] at 635. See also section B.1 [Director82] at 635-36.
16. A process as defined in claim 15 wherein said step of generating data paths comprises applying to the selected cells a set of data path rules stored in a knowledge base and generating the data paths therefrom.	"The Design Automation Assistant is a knowledge-based expert-system, KBES, that generates a technology-independent list of operators, registers, data paths and control signals from an algorithmic description of a VLSI system." [Kowalski85a] at 252; see also [Kowalski83b] at 186 and [Kowalski83a] at 479. "Our approach seeks to aid the designer with tools that automatically produce data paths and control sequences from an algorithmic system description within user-specified constraints". [Kowalski85c] at 33. "The DAA is a knowledge-based expert system that uses a database of over 500 rules to synthesize an architectural implementation from an algorithmic description with constraints. The description is written in ISPS". [Kowalski85c] at 36. "The knowledge-based expert system approach followed by the DAA uses a weak method, match [an inference engine methodology], in place of extensive backtracking." [Kowalski85c] at 36. "The DAA allocates the clock phases, operators, registers, data paths and control logic in two subtasks, dataflow allocation and module allocation, which are shown in Figure 1. This allows the DAA to gather all the information about register usage in the dataflow allocation and then allocate registers and modules in the module allocation. The 55 dataflow allocation rules assign operators to control phases, determine the minimum size needed to represent an operation, allocate temporary registers, and then associate the dataflow operations to register modules or create ALU modules." [Kowalski85a] at 253. "The data-path floor planner (DP): a knowledge-based expert system that is responsible for the complete physical design of the chip. It arranges the

	modules selected by the module binder and control allocator into a data-path floor plan and creates the cell-layout parameters." [Kowalski85c] at 35.
17. A process as defined in claim 16 including the further step of generating control paths for the selected integrated circuit hardware cells.	"Our approach seeks to aid the designer with tools that automatically produce data paths and control sequences from an algorithmic system description within user-specified constraints". [Kowalski85c] at 33. "ISPS describes … the behavior of the hardware units… The behavioral aspects of the unit are described by procedures which specify the sequence of control and data operations in the machine". [Barbacci81] at 25. "DAA … adds register, operator, data path and control signal detail to the VT description [algorithmic level] of hardware to form the SCS description. [technology-independent level". [Kowalski85b] at 5. "The DAA produces a technology-independent hardware network description. This description is composed of modules, ports, links, and a symbolic microcode [i.e. controller]. The modules can be registers, operators, memories, and buses or multiplexers with input, output, and bidirectional ports. The ports are connected by links and are controlled by symbolic microcode." [Kowalski85b] at 26. "The control specification describes the control sequences that govern the behavior of the network." [Kowalski85b] at 56. "Next a controller module is created for the design. The DAA currently has only rules that create single controller designs." [Kowalski85b] at 70. "The Design Automation Assistant is a knowledge-based expert-system, KBES, that generates a technology-independent list of operators, registers, data paths and control signals from an algorithmic description of a VLSI system." [Kowalski85a] at 252; see also [Kowalski83b] at 186 and [Kowalski83a] at 479. "This algorithmic description is then transformed into a technology-independent network … and a symbolic control description. This network is used to synthesize a technology-dependent network that includes implementations of the technology-independent modules and the controller in the target technology." [Kowalski85c] at 34. "The control allocator: an algorithmic program that designs the controller for the data-path logic designed by the DAA…" [Kowalski85c] at 35. "The control allocator translates the technology-independent control specification, generated by the DAA, into a controller implementation in a chosen technology." [Kowalski85c] at 37. "The control allocator receives information from the technology-dependent hardware network and the module database [i.e. hardware cells] to produce an output file for a specific style of controller." [Kowalski85c]

	at 37.

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

BEFORE THE HONORABLE MARTIN J. JENKINS, JUDGE

SYNOPSYS, INC., PLAINTIFF, VS. RICOH COMPANY, LTD., DEFENDANT.	NO. C 03-2289 MJJ WEDNESDAY, DECEMBER 15, 2004 SAN FRANCISCO, CALIFORNIA
RICOH COMPANY, PLAINTIFF, VS. AEROFLEX, INC. ET AL., DEFENDANTS.	C 03-4669 MJJ WEDNESDAY, DECEMBER 15, 2004 SAN FRANCISCO, CALIFORNIA

REPORTER'S TRANSCRIPT OF PROCEEDINGS

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OFFICIAL COURT REPORTER

MACRO AND WHAT YOU INITIALLY PUT IN SO YOU CAN MAKE SOME ADJUSTMENTS THAT SIMULATES WHAT YOU'VE ASKED FOR IN A WAY THAT IT ALLOWS YOU TO FURTHER USE THE EDITOR?

MR. HOFFMAN: YES.

IN THE PREFERRED EMBODIMENT, IT WOULD ALLOW YOU TO GO BACK AND MODIFY IT, GO BACK AND CHECK IT. DOES IT MAKE SENSE? DOES IT LOOK RIGHT? DO I WANT TO CHANGE ANYTHING? I WANT TO DO IT DIFFERENTLY. I WANT IT TO ASSOCIATE IT WITH SOMETHING ELSE. I HAVE AN EDITING-TYPE FUNCTION. OF COURSE, OBVIOUSLY, I CAN GO BACK AND CHECK IT ALSO.

BUT WHAT THE DEFINITIONS ARE, THE SET OF DEFINITIONS -- AND WE HAVE STAYED WITH THE WORD "DEFINITIONS" INSTEAD OF SWITCHING IT. OF COURSE, QUITE CANDIDLY, I THINK DEFINITIONS IS AN EVERYDAY TERM AND IT SEEMED CLEAR ON ITS ORDINARY MEANING AND NOT NEEDING A SEPARATE INTERPRETATION.

BUT IT IS THE LIBRARY OF MACROS OF THE DIFFERENT ARCHITECTURE INDEPENDENT ACTIONS AND CONDITIONS. WHERE THE PRIMARY DIFFERENCE IS BETWEEN US AND THE DEFENDANTS IS THE ISSUES OF FLOWCHART AND RTL, AGAIN, IS WHERE THE DISTINCTIONS COME IN.

IN FACT, I BELIEVE THAT IN THEIR INTERPRETATION, WHILE THEY DON'T USE THE WORD "DEFINITIONS," THEY REFER TO DEFINING. AGAIN, THE WORD DEFINE BEING THE ROOT THAT'S UTILIZED IN BOTH OF THE INTERPRETATIONS.

LET ME BRIEFLY SKIP OVER THE EXPERT SYSTEM KNOWLEDGE

WEBSTER'S Ninth New Collegiate Dictionary

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Library of Congress Cataloging in Publication Data
Main entry under title:

Webster's ninth new collegiate dictionary.

Includes index.
1. English language—Dictionaries. I. Merriam-Webster Inc.
PE1628.W5638 1988 423 87-24041
ISBN 0-87779-508-8
ISBN 0-87779-509-6 (indexed)
ISBN 0-87779-510-X (deluxe)

Made in the United States of America

27282930RMcN88

CATE ⟨rigidly *defined* property lines⟩ **b** : to make distinct, clear, or detailed in outline ⟨the issues aren't too well *defined*⟩ **3** : CHARACTERIZE, DISTINGUISH ⟨you ~ yourself by the choices you make —*Denison Univ. Bull.*⟩ ~ *vi* : to make a definition — **de·fin·able** \-'fī-nə-bəl\ *adj* — **de·fin·ably** \-blē\ *adv* — **de·fine·ment** \-'fīn-mənt\ *n* — **de·fin·er** \-'fī-nər\ *n*

de·fin·i·en·dum \di-ˌfin-ē-'en-dəm\ *n, pl* **-da** \-də\ [L, something to be defined, neut. of *definiendus*, gerundive of *definire*] (1871) : an expression that is being defined

de·fin·i·ens \di-'fin-ē-ˌenz\ *n, pl* **de·fin·i·en·tia** \di-ˌfin-ē-'en-ch(ē-)ə\ [L, prp. of *definire*] (1871) : an expression that defines : DEFINITION

def·i·nite \'def-(ə-)nət\ *adj* [L *definitus*, pp. of *definire*] (1553) **1** : having distinct or certain limits ⟨set ~ standards for pupils to meet⟩ **2 a** : free of all ambiguity, uncertainty, or obscurity ⟨demanded a ~ answer⟩ **b** : UNQUESTIONABLE, DECIDED ⟨the quarterback was a ~ hero today⟩ **3** : typically designating an identified or immediately identifiable person or thing ⟨the ~ article *the*⟩ **4 a** : being constant in number, usu. less than 20, and occurring in multiples of the petal number ⟨stamens ~⟩ **b** : CYMOSE *syn* see EXPLICIT — **def·i·nite·ly** *adv* — **def·i·nite·ness** *n*

definite integral *n* (1860) : a number that is the difference between the values of the indefinite integral of a given function for two values of the independent variable

def·i·ni·tion \ˌdef-ə-'nish-ən\ *n* [ME *diffinicioun*, fr. MF *definition*, fr. L *definition-*, *definitio*, fr. *definitus*, pp.] (14c) **1** : an act of determining; *specif* : the formal proclamation of a Roman Catholic dogma **2 a** : a statement expressing the essential nature of something (as by differentiation within a class) **b** : a statement of the meaning of a word or word group or a sign or symbol ⟨dictionary ~s⟩ **c** : a product of defining **3** : the action or process of stating or formulating a definition **4 a** : the action or the power of describing, explaining, or making definite and clear ⟨the ~ of a telescope⟩ ⟨her comic genius is beyond ~⟩ **b** (1) : distinctness of outline or detail (as in a photograph) (2) : clarity esp. of musical sound in reproduction **c** : sharp demarcation of outlines or limits ⟨a jacket with definite waist ~⟩ — **def·i·ni·tion·al** \-'nish-nəl, -'nish-ən-ᵊl\ *adj*

¹de·fin·i·tive \di-'fin-ət-iv\ *adj* [ME *diffinityf*, fr. MF *definitif*, fr. L *definitivus*, fr. *definitus*] (14c) **1** : serving to provide a final solution ⟨a ~ victory⟩ **2** : authoritative and apparently exhaustive ⟨a ~ biography⟩ **3** : serving to define or specify precisely ⟨~ laws⟩ **4** : fully differentiated or developed **5** *of a postage stamp* : issued as a regular stamp for the country or territory in which it is to be used *syn* see CONCLUSIVE — **de·fin·i·tive·ly** *adv* — **de·fin·i·tive·ness** *n*

²definitive *n* (1951) : a definitive postage stamp — compare PROVISIONAL

definitive host *n* (1901) : the host in which the sexual reproduction of a parasite takes place

de·fi·ni·tize \'def-(ə-)nə-ˌtīz, di-'fin-ə-\ *vt* **-tized; -tiz·ing** (1876) : to make definite

de·fi·ni·tude \di-'fin-ə-ˌt(y)üd, -'fī-nə-\ *n* [irreg. fr. *definite*] (1836) : PRECISION, DEFINITENESS

def·la·grate \'def-lə-ˌgrāt\ *vb* **-grat·ed; -grat·ing** [L *deflagratus*, pp. of *deflagrare* to burn down, fr. *de-* + *flagrare* to burn — more at BLACK] *vt* (1727) : to cause to deflagrate — compare DETONATE ~ *vi* : to burn rapidly with intense heat and sparks being given off — **def·la·gra·tion** \ˌdef-lə-'grā-shən\ *n*

de·flate \di-'flāt, 'dē-\ *vb* **de·flat·ed; de·flat·ing** [*de-* + *-flate* (as in *inflate*)] *vt* (1891) **1** : to release air or gas from **2** : to reduce in size or importance ⟨~ his ego with cutting remarks⟩ **3** : to reduce ⟨a price level⟩ or cause ⟨a volume of credit⟩ to contract ~ *vi* : to lose firmness through or as if through the escape of contained gas *syn* see CONTRACT — **de·fla·tor** \-'flāt-ər\ *n*

de·fla·tion \di-'flā-shən, 'dē-\ *n* (1891) **1** : an act or instance of deflating ; the state of being deflated **2** : a contraction in the volume of available money or credit that results in a decline of the general price level **3** : the erosion of soil by the wind — **de·fla·tion·ary** \-shə-ˌner-ē\ *adj*

de·flect \di-'flekt\ *vb* [L *deflectere* to bend down, turn aside, fr. *de-* + *flectere* to bend] *vt* (1555) : to turn from a straight course or fixed direction : BEND ~ *vi* : to turn aside : DEVIATE — **de·flect·able** \-'flek-tə-bəl\ *adj* — **de·flec·tive** \-tiv\ *adj* — **de·flec·tor** \-tər\ *n*

de·flec·tion \di-'flek-shən\ *n* (1605) **1** : a turning aside or off course : DEVIATION **2** : the departure of an indicator or pointer from the zero reading on the scale of an instrument

de·flexed \dē-,flekst, di-'\ *adj* [L *deflexus*, pp. of *deflectere*] (1826) : turned abruptly downward ⟨a ~ leaf⟩

de·flo·ra·tion \ˌdef-lə-'rā-shən, ˌdē-flə-\ *n* [ME *defloracioun*, fr. LL *defloration-*, *defloratio*, fr. *defloratus*, pp. of *deflorare*] (15c) : rupture of the hymen

de·flow·er \(')dē-'flau̇(-ə)r\ *vt* [ME *deflouren*, fr. MF or LL; MF *deflorer*, fr. LL *deflorare*, fr. L *de-* + *flor-*, *flos* flower — more at BLOW] (14c) **1** : to deprive of virginity : RAVISH **2** : to take away the prime beauty of — **de·flow·er·er** *n*

de·foam \(')dē-'fōm\ *vt* (1939) : to remove foam from : prevent the formation of foam in — **de·foam·er** *n*

de·fog \(')dē-'fȯg, -'fäg\ *vt* (1904) : to remove fog or condensed moisture from — **de·fog·ger** *n*

de·fo·li·ant \(')dē-'fō-lē-ənt\ *n* (1943) : a chemical spray or dust applied to plants in order to cause the leaves to drop off prematurely

de·fo·li·ate \-lē-ˌāt\ *vt* [LL *defoliatus*, pp. of *defoliare*, fr. L *de-* + *folium* leaf — more at BLADE] (1791) : to deprive of leaves esp. prematurely — **de·fo·li·a·tion** \(ˌ)dē-ˌfō-lē-'ā-shən\ *n* — **de·fo·li·a·tor** \(')dē-'fō-lē-ˌāt-ər\ *n*

de·force \(')dē-'fō(ə)rs, -'fȯ(ə)rs\ *vt* [ME *deforcen*, fr. MF *deforcier*, fr. *de-* + *forcier* to force] (15c) **1** : to keep (as lands) by force from the rightful owner **2** : to eject (a person) from possession by force — **de·force·ment** \-'fōr-smənt, -'fȯr-\ *n*

de·for·ciant \di-'fōr-shənt, -'fȯr-\ *n* [AF, fr. OF, prp. of *deforcier*] (15c) : one who deforces the rightful owner

de·for·es·ta·tion \(ˌ)dē-ˌfȯr-ə-'stā-shən, -ˌfär-\ *n* (1874) : the action or process of clearing of forests; *also* : the state of having been cleared of forests — **de·for·est** \(')dē-'fȯr-əst, -'fär-\ *vt*

de·form \di-'fȯ(ə)rm, 'dē-\ *vb* [ME *deformen*, fr. MF or L; MF *deformer*, fr. L *deformare*, fr. *de-* + *formare* to form, fr. *forma* form] *vt* (15c) **1** : to spoil the form of **2 a** : to spoil the looks of : DISFIGURE ⟨a face ~*ed* by bitterness⟩ **b** : to make hideous or monstrous **3** : to alter the shape of by stress ~ *vi* : to become misshapen or changed in shape *syn* DEFORM, DISTORT, CONTORT, WARP mean to mar or spoil by or as if by twisting. DEFORM may imply a change of shape through stress, injury, or some accident of growth; DISTORT and CONTORT both imply a wrenching from the natural, normal, or justly proportioned, but CONTORT suggests a more involved twisting and a more grotesque and painful result; WARP indicates physically an uneven shrinking that bends or twists out of a flat plane.

de·for·mal·ize \(')dē-'fȯr-mə-ˌlīz\ *vt* (1880) : to make less formal

de·for·ma·tion \ˌdē-ˌfȯr-'mā-shən, ˌdef-ər-\ *n* (15c) **1** : alteration of form or shape; *also* : the product of such alteration **2** : the action of deforming ; the state of being deformed **3** : change for the worse — **de·for·ma·tion·al** \-shnəl, -shən-ᵊl\ *adj*

de·for·ma·tive \di-'fȯr-mət-iv\ *adj* (1641) : tending to deform

de·formed *adj* (15c) : distorted or unshapely in form : MISSHAPEN

de·for·mi·ty \di-'fȯr-mət-ē\ *n, pl* **-ties** [ME *deformite*, fr. MF *deformité*, fr. L *deformitat-*, *deformitas*, fr. *deformis* deformed, fr. *de-* + *forma*] (15c) **1** : the state of being deformed **2** : a physical blemish or distortion : DISFIGUREMENT **3** : a moral or aesthetic flaw or defect

de·fraud \di-'frȯd\ *vt* [ME *defrauden*, fr. MF *defrauder*, fr. L *defraudare*, fr. *de-* + *fraudare* to cheat, fr. *fraud-*, *fraus* fraud] (14c) : to deprive of something by deception or fraud *syn* see CHEAT — **de·fraud·er** \-'frȯd-ər\ *n*

de·fray \di-'frā\ *vt* [MF *desfrayer*, fr. *des-* de- + *frayer* to expend, fr. OF, fr. (assumed) OF *frai* expenditure, lit., damage by breaking, fr. L *fractum*, neut. of *fractus*, pp. of *frangere* to break — more at BREAK] (1543) **1** : to provide for the payment of : PAY **2** *archaic* : to bear the expenses of — **de·fray·able** \-ə-bəl\ *adj* — **de·fray·al** \-'frā(-ə)l\ *n*

de·frock \(')dē-'fräk\ *vt* (1581) : UNFROCK

de·frost \di-'frȯst, 'dē-\ *vt* (1895) **1** : to release from a frozen state ⟨~ meat⟩ **2** : to free from ice ⟨~ the refrigerator⟩ ~ *vi* : to thaw out esp. from a deep-frozen state — **de·frost·er** *n*

deft \'deft\ *adj* [ME *defte*] (15c) : marked by facility and skill *syn* see DEXTEROUS — **deft·ly** *adv* — **deft·ness** \'def(t)-nəs\ *n*

de·funct \di-'fəŋ(k)t\ *adj* [L *defunctus*, fr. pp. of *defungi* to finish, die, fr. *de-* + *fungi* to perform — more at FUNCTION] (1599) : having finished the course of life or existence ⟨her ~ aunt's will⟩ ⟨the committee is now ~⟩ *syn* see DEAD

de·fuse \(')dē-'fyüz\ *vt* (1943) **1** : to remove the fuse from ⟨as a mine or bomb⟩ **2** : to make less harmful, potent, or tense : CALM ⟨~ the crisis⟩

¹de·fy \di-'fī\ *vt* **de·fied**; **de·fy·ing** [ME *defyen* to renounce faith in, challenge, fr. MF *defier*, fr. *de-* + *fier* to entrust, fr. (assumed) VL *fidare*, alter. of L *fidere* to trust — more at BIDE] (14c) **1** *archaic* : to challenge to combat **2** : to challenge to do something considered impossible : DARE **3** : to confront with assured power of resistance : DISREGARD ⟨~ public opinion⟩ **4** : to resist attempts at : WITHSTAND ⟨the paintings ~ classification⟩

²de·fy \di-'fī, 'dē-\ *n, pl* **defies** (1580) : CHALLENGE, DEFIANCE

dé·ga·gé \ˌdā-ˌgä-'zhā\ *adj* [F, fr. pp. of *dégager* to redeem a pledge, free, fr. OF *desgagier*, fr. *des-* de- + *gage* pledge — more at GAGE] (1696) **1** : free of constraint : NONCHALANT **2** : being free and easy ⟨clothes with a ~ look⟩ **3** : extended with toe pointed in preparation for a ballet step

de·gas \(')dē-'gas\ *vt* (1920) : to remove gas from ⟨~ an electron tube⟩

de Gaul·lism \di-'gō-ˌliz-əm, -'gȯ-\ *n* (1943) : GAULLISM — **de Gaul·list** \-ləst\ *n*

de·gauss \(')dē-'gau̇s\ *vt* [*de-* + *gauss*, after Karl F. *Gauss*] (ca. 1940) **1** : to make (a steel ship) effectively nonmagnetic by means of electrical coils carrying currents that neutralize the magnetism of the ship **2** : DEMAGNETIZE — **de·gauss·er** *n*

de·gen·er·a·cy \di-'jen-(ə-)rə-sē\ *n, pl* **-cies** (1664) **1** : the state of being degenerate **2** : the process of becoming degenerate **3** : sexual perversion **4** : the coding of an amino acid by more than one codon of the genetic code

¹de·gen·er·ate \di-'jen-(ə-)rət\ *adj* [ME *degenerat*, fr. L *degeneratus*, pp. of *degenerare* to degenerate, fr. *de-* + *gener-*, *genus* race, kind — more at KIN] (15c) **1 a** : having declined (as in nature, character, structure or function) from an ancestral or former state **b** : having sunk to a condition below that which is normal to a type; *esp* : having sunk to a lower and usu. peculiarly corrupt and vicious state **c** : DEGRADED **2** : being mathematically simpler (as by having a factor or constant equal to zero) than the typical case ⟨the graph of a second degree equation yielding two intersecting lines is a ~ hyperbola⟩ **3** : characterized by atoms stripped of their electrons and by very great density ⟨~ matter⟩; *also* : consisting of degenerate matter ⟨a ~ star⟩ **4 a** : having two or more states or subdivisions ⟨~ energy level⟩ **b** *of a semiconductor* : having a sufficient concentration of impurities to conduct electricity **5** : having more than one codon representing an amino acid; *also* : being such a codon *syn* see VICIOUS — **de·gen·er·ate·ly** *adv* — **de·gen·er·ate·ness** *n*

²de·gen·er·ate \di-'jen-ə-ˌrāt\ *vi* (1545) **1** : to pass from a higher to a lower type or condition : DETERIORATE **2** : to sink into a low intellectual or moral state **3** : to decline in quality ⟨his poetry gradually *degenerated* into jingles⟩ **4** : to decline from a condition or from the standards of a species, race, or breed **5** : to evolve or develop into a less autonomous or less functionally active form ⟨*degenerated* into dependent parasites⟩ ⟨the digestive system *degenerated*⟩ ~ *vt* : to cause to degenerate

³de·gen·er·ate \di-'jen-(ə-)rət\ *n* (1555) : one that is degenerate: as **a** : one degraded from the normal moral standard **b** : a sexual pervert **c** : one showing signs of reversion to an earlier culture stage

de·gen·er·a·tion \di-ˌjen-ə-'rā-shən, ˌdē-\ *n* (15c) **1** : degenerate condition **2** : a lowering of effective power, vitality, or essential quality in an enfeebled and worsened kind or state **3** : intellectual or moral decline **4 a** : progressive deterioration of physical characters from a level representing the norm of earlier generations or forms **b** : deterioration of a tissue or an organ in which its function is diminished or its structure is impaired **5** : marked decline in excellence (as of workmanship or originality) *syn* see DETERIORATION

WEBSTER'S Ninth New Collegiate Dictionary

²**libel** *vb* **-beled** *or* **-belled; -bel·ing** *or* **-bel·ling** \-b(ə-)liŋ\ *vi* (1570) : to make libelous statements ~ *vt* : to make or publish a libel against — **li·bel·er** \-b(ə-)lər\ *n* — **li·bel·ist** \-bə-ləst\ *n*

li·bel·ant *or* **li·bel·lant** \'lī-bə-lənt\ *n* (1726) : one that institutes a suit by a libel

li·bel·ee *or* **li·bel·lee** \,lī-bə-'lē\ *n* (1856) : one against whom a libel has been filed in a court

li·bel·ous *or* **li·bel·lous** \'lī-b(ə-)ləs\ *adj* (1619) : constituting or including a libel : DEFAMATORY ⟨a ~ statement⟩

Li·be·ra \'lē-bə-,rä, 'lē-brə\ *n* [L, lit., deliver, imper. of *liberare* to liberate; fr. the first word of the responsory] (ca. 1903) : a Roman Catholic funeral responsory

¹**lib·er·al** \'lib(-ə)-rəl\ *adj* [ME, fr. MF, fr. L *liberalis* suitable for a freeman, generous, fr. *liber* free; akin to OE *lēodan* to grow, Gk *eleutheros* free] (14c) **1 a** : of, relating to, or based on the liberal arts ⟨~ education⟩ **b** *archaic* : of or befitting a man of free birth **2 a** : GENEROUS, OPENHANDED ⟨a ~ giver⟩ **b** : given or provided in a generous and openhanded way ⟨a ~ meal⟩ **c** : AMPLE, FULL **3** *obs* : lacking moral restraint : LICENTIOUS **4** : not literal or strict : LOOSE ⟨a ~ translation⟩ **5** : BROAD-MINDED; *esp* : not bound by authoritarianism, orthodoxy, or traditional forms **6 a** : of, favoring, or based upon the principles of liberalism **b** *cap* : of or constituting a political party advocating or associated with the principles of political liberalism; *esp* : of or constituting a political party in the United Kingdom associated with ideals of individual esp. economic freedom, greater individual participation in government, and constitutional, political, and administrative reforms designed to secure these objectives — **lib·er·al·ly** \-rə-lē\ *adv* — **lib·er·al·ness** *n*

syn LIBERAL, GENEROUS, BOUNTIFUL, MUNIFICENT mean giving freely and unstintingly. LIBERAL suggests openhandedness in the giver and largeness in the thing or amount given; GENEROUS stresses warmhearted readiness to give more than size or importance of the gift; BOUNTIFUL suggests lavish, unremitting giving or providing; MUNIFICENT suggests a scale of giving appropriate to lords or princes.

²**liberal** *n* (1816) : one who is liberal: as **a** : one who is open-minded or not strict in the observance of orthodox, traditional or established forms or ways **b** *cap* : a member or supporter of a liberal political party **c** : an advocate or adherent of liberalism esp. in individual rights

liberal arts *n pl* (14c) **1** : the medieval studies comprising the trivium and quadrivium **2** : the studies (as language, philosophy, history, literature, abstract science) in a college or university intended to provide chiefly general knowledge and to develop the general intellectual capacities (as reason and judgment) as opposed to professional or vocational skills

lib·er·al·ism \'lib(-ə)-rə-,liz-əm\ *n* (1819) **1** : the quality or state of being liberal **2 a** *often cap* : a movement in modern Protestantism emphasizing intellectual liberty and the spiritual and ethical content of Christianity **b** : a theory in economics emphasizing individual freedom from restraint and usu. based on free competition, the self-regulating market, and the gold standard **c** : a political philosophy based on belief in progress, the essential goodness of man, and the autonomy of the individual and standing for the protection of political and civil liberties **d** *cap* : the principles and policies of a Liberal party — **lib·er·al·ist** \-rə-ləst\ *n or adj* — **lib·er·al·is·tic** \,lib(-ə)-rə-'lis-tik\ *adj*

lib·er·al·i·ty \,lib-ə-'ral-ət-ē\ *n, pl* **-ties** (14c) : the quality or state of being liberal; *also* : an instance of this

lib·er·al·ize \'lib(-ə)-rə-,līz\ *vb* **-ized; -iz·ing** *vt* (1774) : to make liberal or more liberal ~ *vi* : to become liberal or more liberal — **lib·er·al·iza·tion** \,lib(-ə)-rə-lə-'zā-shən\ *n* — **lib·er·al·iz·er** \'lib(-ə)-rə-,lī-zər\ *n*

lib·er·ate \'lib-ə-,rāt\ *vt* **-at·ed; -at·ing** [L *liberatus*, pp. of *liberare*, fr. *liber*] (ca. 1623) **1** : to set at liberty : FREE; *specif* : to free (as a country) from domination by a foreign power **2** : to free from combination ⟨~ the gas by adding acid⟩ **3** : to take or take over illegally or unjustly ⟨a . . . barricade was constructed . . . with material *liberated* from a nearby construction site —Thorne Dreyer⟩ *syn* see FREE — **lib·er·a·tor** \-,āt-ər\ *n*

lib·er·at·ed *adj* (1946) : freed from or opposed to traditional social and sexual attitudes or roles ⟨a ~ woman⟩ ⟨a ~ marriage⟩

lib·er·a·tion \,lib-ə-'rā-shən\ *n* (15c) **1** : the act of liberating : the state of being liberated **2** : a movement seeking equal rights and status for a group ⟨women's ~⟩ — **lib·er·a·tion·ist** \-sh(ə-)nəst\ *n*

lib·er·tar·i·an \,lib-ər-'ter-ē-ən\ *n* (1789) **1** : an advocate of the doctrine of free will **2** : one who upholds the principles of absolute and unrestricted liberty esp. of thought and action — **libertarian** *adj* — **lib·er·tar·i·an·ism** \-ē-ə-,niz-əm\ *n*

lib·er·tin·age \'lib-ər-,tē-nij\ *n* (1611) : LIBERTINISM

¹**lib·er·tine** \'lib-ər-,tēn\ *n* [ME *libertyn*, freedman, fr. L *libertinus*, fr. *libertinus*, adj., of a freedman, fr. *libertus* freedman, fr. *liber*] (1563) **1** : a freethinker esp. in religious matters — usu. used disparagingly **2** : a person who is unrestrained by convention or morality; *specif* : one leading a dissolute life

²**libertine** *adj* (1577) : of, relating to, or characteristic of a libertine

lib·er·tin·ism \'lib-ər-,tē-,niz-əm, -tə-\ *n* (1611) : the quality or state of being libertine : the behavior of a libertine

lib·er·ty \'lib-ərt-ē\ *n, pl* **-ties** [ME, fr. MF *liberté*, fr. L *libertat-, libertas*, fr. *liber* free — more at LIBERAL] (14c) **1** : the quality or state of being free: **a** : the power to do as one pleases **b** : freedom from physical restraint **c** : freedom from arbitrary or despotic control **d** : the positive enjoyment of various social, political, or economic rights and privileges **e** : the power of choice **2 a** : a right or immunity enjoyed by prescription or by grant : PRIVILEGE **b** : permission esp. to go freely within specified limits **3** : an action going beyond normal limits: as **a** : a breach of etiquette or propriety : FAMILIARITY **b** : RISK, CHANCE ⟨took foolish *liberties* with his health⟩ **c** : a violation of rules or a deviation from standard practice **d** : a distortion of fact **4** : a short authorized absence from naval duty usu. for less than 48 hours *syn* see FREEDOM — **at liberty** **1** : FREE **2** : at leisure : UNOCCUPIED

liberty cap *n* (1803) : a close-fitting conical cap used as a symbol of liberty by the French revolutionists and in the U.S. before 1800

liberty pole *n* (1770) : a tall flagstaff surmounted by a liberty cap or the flag of a republic and set up as a symbol of liberty

li·bid·i·nal \lə-'bid-ᵊn-əl, -'bid-nᵊl\ *adj* (1922) : of or relating to the libido — **li·bid·i·nal·ly** \-ē\ *adv*

li·bid·i·nous \-ᵊn-əs, -'bid-nəs\ *adj* [ME, fr. MF *libidineus*, fr. L *libidinosus*, fr. *libidin-, libido*] (15c) **1** : having or marked by lustful desires : LASCIVIOUS **2** : LIBIDINAL — **li·bid·i·nous·ly** *adv* — **li·bid·i·nous·ness** *n*

li·bi·do \lə-'bēd-(,)ō, 'lib-ə-,dō\ *n, pl* **-dos** [NL *libidin-, libido*, fr. L, desire, lust, fr. *libēre* to please — more at LOVE] (1909) **1** : emotional or psychic energy that in psychoanalytic theory is derived from primitive biological urges and that is usu. goal-directed **2** : sexual drive

li·bra *for 1 & 2a* 'lē-brə *or* 'lī-brə, *for 2b* 'lē-brə *or* 'lēv-rə\ *n* [ME, fr. L (gen. *Librae*), lit., scales, pound] **1** *cap* **a** : a southern zodiacal constellation between Virgo and Scorpio represented by a pair of scales **b** (1) : the 7th sign of the zodiac in astrology — see ZODIAC table (2) : one born under this sign **2 a** *pl* **li·brae** \'lī-,brē, 'lē-,brī\ [L] : an ancient Roman unit of weight equal to 327.45 grams **b** [Sp & Pg, fr. L] : any of various Spanish, Portuguese, Colombian, or Venezuelan units of weight

Li·bran \'lē-brən, 'lī-\ *n* (1967) : LIBRA 1b(2)

li·brar·i·an \lī-'brer-ē-ən\ *n* (1713) : a specialist in the care or management of a library — **li·brar·i·an·ship** \-,ship\ *n*

li·brary \'lī-,brer-ē; *Brit usu & US sometimes* -brər-ē; *US sometimes* -brē, -ˌber-ē\ *n, pl* **-brar·ies** [ME, fr. ML *librarium*, fr. L, neut. of *librarius* of books, fr. *libr-, liber* book — more at LEAF] (14c) **1 a** : a place in which literary, musical, artistic, or reference materials (as books, manuscripts, recordings, or films) are kept for use but not for sale **b** : a collection of such materials **2 a** : a collection resembling or suggesting a library ⟨a ~ of computer programs⟩ ⟨wine ~⟩ **b** : MORGUE **3 a** : a series of related books issued by a publisher **b** : a collection of publications on the same subject

usage While the pronunciation \'lī-,brer-ē\ is the most frequent variant in the U.S., the other variants are not uncommon. The contraction \'lī-brē\ and the dissimilated form \'lī-,ber-ē\ result from the relative difficulty of repeating \r\ in successive syllables and are heard from educated speakers, including college presidents and professors, as well as with somewhat greater frequency from less educated speakers.

library paste *n* (1953) : a thick white adhesive made from starch

library science *n* (1902) : the study or the principles and practices of library care and administration

li·bra·tion \lī-'brā-shən\ *n* [L *libration-, libratio*, fr. *libratus*, pp. of *librare* to balance, fr. *libra* scales] (1669) : an oscillation in the apparent aspect of a secondary body (as a planet or a satellite) as seen from the primary object around which it revolves — **li·bra·tion·al** \-shnəl, -shən-ᵊl\ *adj* — **li·bra·to·ry** \'lī-brə-,tōr-ē, -,tȯr-\ *adj*

li·bret·tist \lə-'bret-əst\ *n* (1862) : the writer of a libretto

li·bret·to \lə-'bret-(,)ō\ *n, pl* **-tos** *or* **-ti** \-(,)ē\ [It, dim. of *libro* book, fr. L *libr-, liber*] (1742) **1** : the text of a work (as an opera) for the musical theater **2** : the book containing a libretto

li·bri·form \'lī-brə-,fȯrm\ *adj* [L *libr-, liber* + ISV *-iform*] (1877) : resembling phloem fibers

Lib·ri·um \'lib-rē-əm\ *trademark* — used for a preparation of chlordiazepoxide

Lib·y·an \'lib-ē-ən\ *n* (1607) **1** : a native or inhabitant of Libya **2** : a Berber language of ancient No. Africa — **Libyan** *adj*

lice *pl of* LOUSE

¹**li·cense** *or* **li·cence** \'līs-ᵊn(t)s\ *n* [ME, fr. MF *licence*, fr. L *licentia*, fr. *licent-, licens*, prp. of *licēre* to be permitted; akin to Latvian *līgt* to come to terms] (14c) **1 a** : permission to act **b** : freedom of action **2 a** : a permission granted by competent authority to engage in a business or occupation or in an activity otherwise unlawful **b** : a document, plate, or tag evidencing a license granted **3 a** : freedom that allows or is used with irresponsibility **b** : disregard for rules of personal conduct : LICENTIOUSNESS **4** : deviation from fact, form, or rule by an artist or writer for the sake of the effect gained *syn* see FREEDOM

²**license** *also* **licence** *vt* **li·censed; li·cens·ing** (15c) **1** : to issue a license to **2** : to permit or authorize esp. by formal license — **li·cens·able** \-ᵊn-sə-bəl\ *adj* — **li·cens·er** \-sər\ *or* **li·cen·sor** \-sər, ˌlīs-ᵊn-'sȯ(ə)r\ *n*

licensed practical nurse *n* (1951) : a person who has undergone training and obtained a license (as from a state) conferring authorization to provide routine care for the sick

li·cens·ee \ˌlīs-ᵊn-'sē\ *n* (1864) : one that is licensed

license plate *n* (1926) : a plate or tag (as of metal) attesting that a license has been secured and usu. bearing a registration number

li·cen·sure \'līs-ᵊn-shər, -ˌshu̇(ə)r\ *n* (ca. 1846) : the granting of licenses esp. to practice a profession

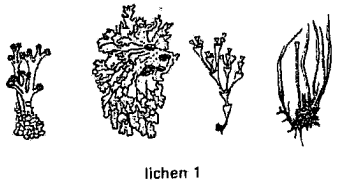
li·cen·te \lə-'sent-ē\ *n, pl* **licente** *or* **li·cen·ti** \-ē\ [native name in Lesotho] (1966) — see *loti* at MONEY table

li·cen·ti·ate \lī-'sen-chē-ət, *esp in sense 2* lī-\ *n* [ML *licentiatus*, fr. pp. of *licentiare* to allow, fr. L *licentia*] (14c) **1** : one who has a license granted esp. by a university to practice a profession **2** : an academic degree ranking below that of doctor given by some European universities

li·cen·tious \lī-'sen-chəs\ *adj* [L *licentiosus*, fr. *licentia*] (1535) **1** : lacking legal or moral restraints; *esp* : disregarding sexual restraints **2** : marked by disregard for strict rules of correctness — **li·cen·tious·ly** *adv* — **li·cen·tious·ness** *n*

li·chee *var of* LITCHI

li·chen \'lī-kən, *Brit also* 'lich-ən\ *n* [L, fr. Gk *leichēn, lichēn*; akin to Gk *leichein* to lick] (1601) **1** : any of numerous complex thallophytic plants (group Lichenes) made up of an alga and a fungus growing in symbiotic association on a solid surface (as a rock) **2** : any of several skin diseases characterized by a papular eruption — **li·chened** \-kənd\ *adj* — **li·chen·ous** \-kə-nəs\ *adj*



lichen 1